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ITRS 2002 Yield Enhancement (YE) Update

Presenters: Toshihiko Osada (Fujitsu) and
Fred Lakhani (International Sematech)

Presentation Outline

- Yield Enhancement (YE) TWG Membership
- YE Difficult Challenges
- Changes in 2002 Electronic Update
- Changes and Additions for 2003
- Summary

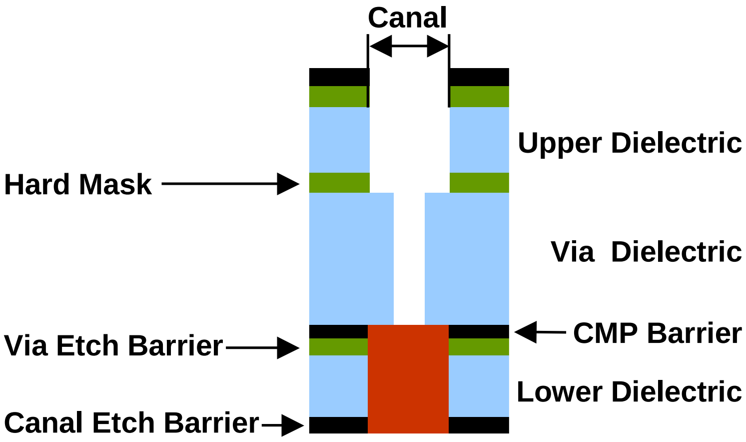
2001 ITRS YE ITWG Co-chairs

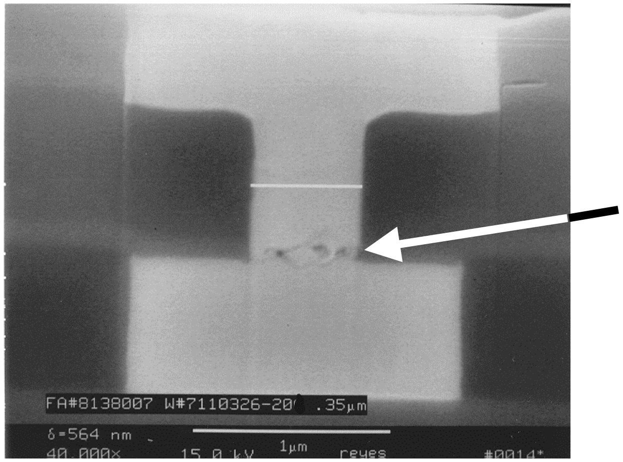
- **Europe**
  - Ines Thurner
    - Infineon
- **Japan**
  - Toshihiko Osada
    - Fujitsu
  - Hiroshi Kitajima
    - Selete
- **Korea**
  - TBD
- **Taiwan**
  - Len Mei
    - Promos Technologies
- **United States**
  - Christopher Long
    - IBM
  - Fred Lakhani
    - International Sematech

YE Difficult Challenges

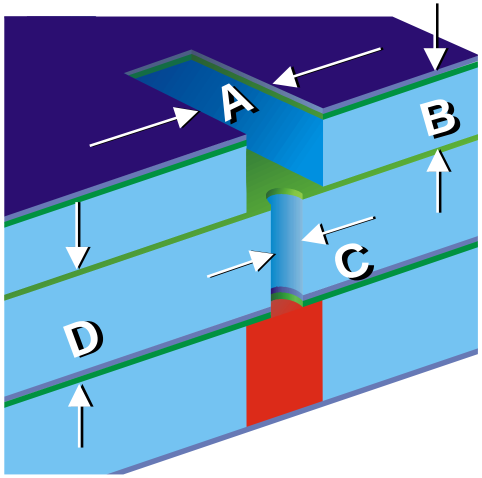
- *High-Aspect-Ratio Inspection*.
  - High-speed, cost-effective tools are needed to rapidly detect defects at 1/2 X ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches and especially defects near or at the bottoms of these features.
- *Non-visual Defect Detection*
  - In-line and end-of-line tools and techniques are needed to detect non-visual defects.
- *Data Management for Rapid Yield Learning*.
  - Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test, and work-in-process (WIP) data must be developed to enable the rapid root-cause analysis of yield-limiting conditions.

High-Aspect Ratio Inspection (HARI)

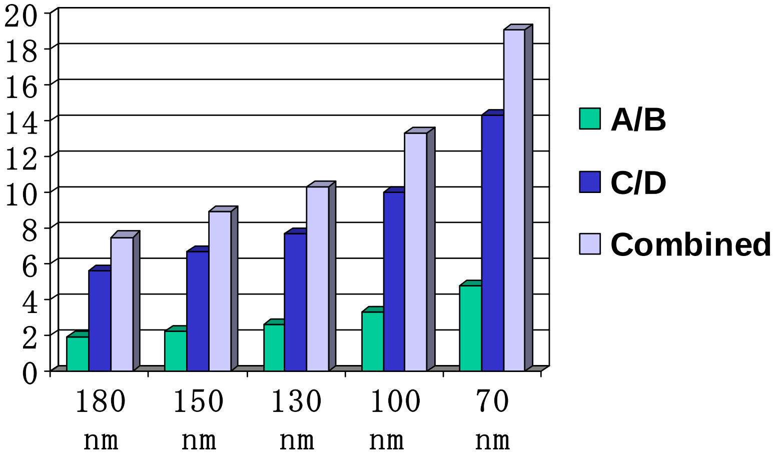




Void
caused by
residue left
behind after
via etch
process
step

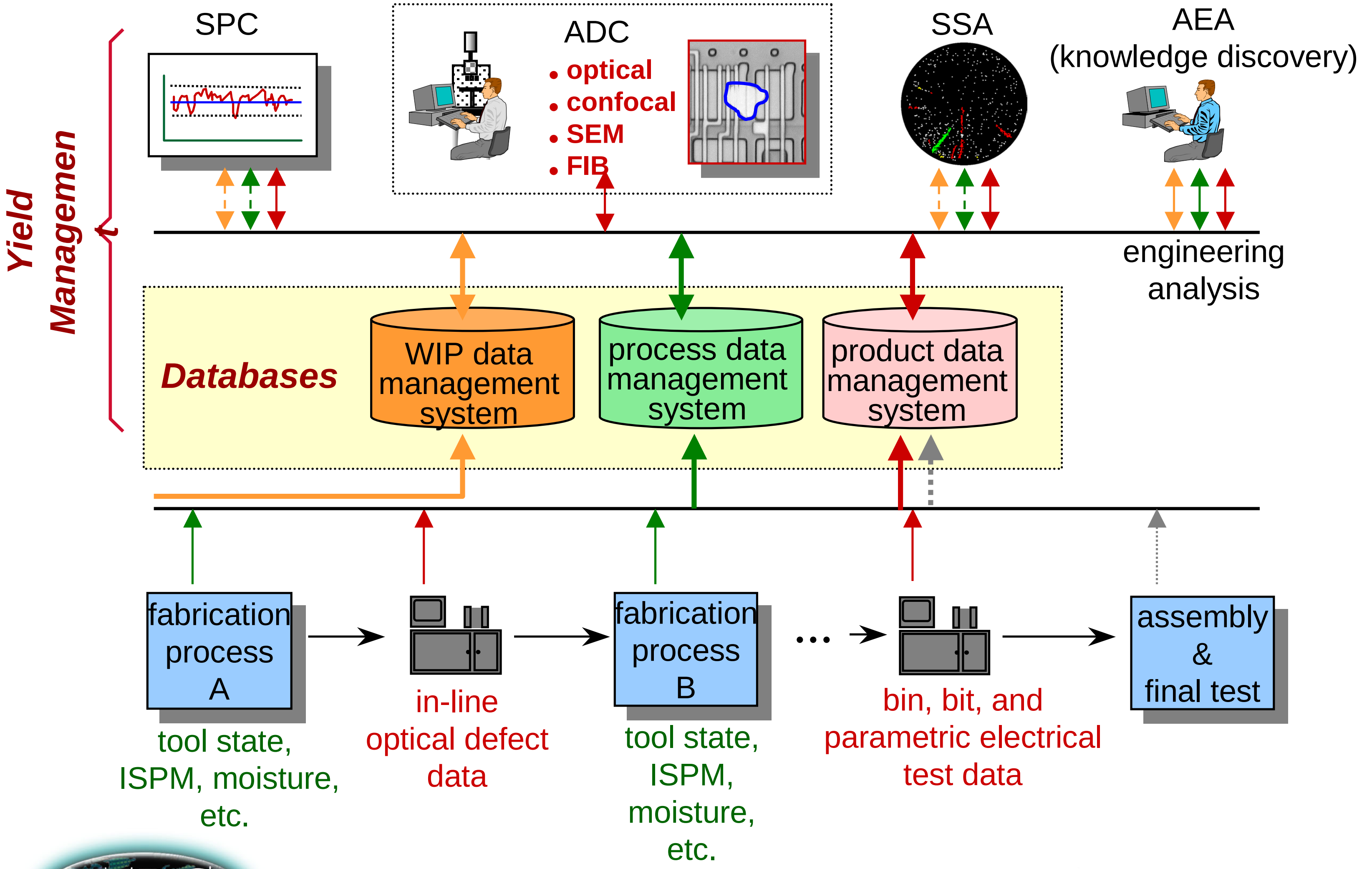


Aspect Ratios at Future NTRS Nodes



Yield Management Today

Increasing Data Complexity



SPC

ADC
- optical
- confocal
- SEM
- FIB

SSA

AEA
(knowledge discovery)

engineering
analysis

Yield Management

Databases

WIP data management system

process data management system

product data management system

fabrication process A

tool state,
ISPM, moisture,
etc.

in-line
optical defect
data

fabrication process B

tool state,
ISPM,
moisture,
etc.

…

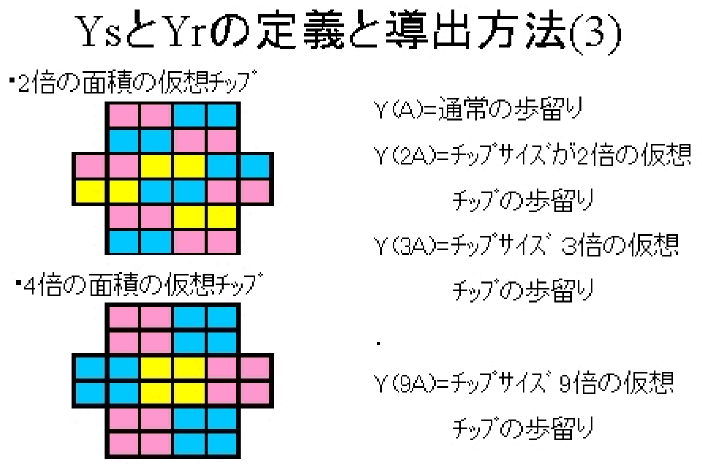
bin, bit, and
parametric electrical
test data

assembly
&
final test

YE Difficult Challenges (continued)

- *Design for Manufacture & Test (DFM & DFT) and Systematic Mechanisms Limited Yield (SMLY)*
  - IC designs must be optimized for a given process capability and must be testable and diagnosable. Understanding SMLY is mandatory for achieving historic yield ramps in the future.
- *Yield Models*
  - Random, systematic, parametric, and memory redundancy models must be developed and validated to correlate process-induced defects (PID), particle counts per wafer pass (PWP), and *in-situ* tool/process measurements to yield.
- *Correlation of Impurity Level to Yield.*
  - Test structures and methods are needed for correlating fluid/gas contamination types and levels to yield.

Ｙｓ：システム歩留



YsとYrの定義と導出方法(3)

・2倍の面積の仮想ﾁｯﾌﾟ

・4倍の面積の仮想ﾁｯﾌﾟ

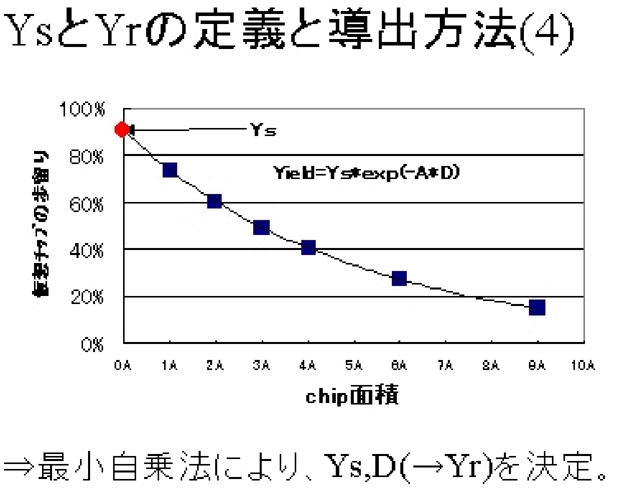
Y(A)=通常の歩留り

Y(2A)=ﾁｯﾌﾟｻｲｽﾞが2倍の仮想ﾁｯﾌﾟの歩留り

Y(3A)=ﾁｯﾌﾟｻｲｽﾞ 3倍の仮想ﾁｯﾌﾟの歩留り

・

Y(9A)=ﾁｯﾌﾟｻｲｽﾞ 9倍の仮想ﾁｯﾌﾟの歩留り



YsとYrの定義と導出方法(4)

⇒最小自乗法により、Ys,D(→Yr)を決定。

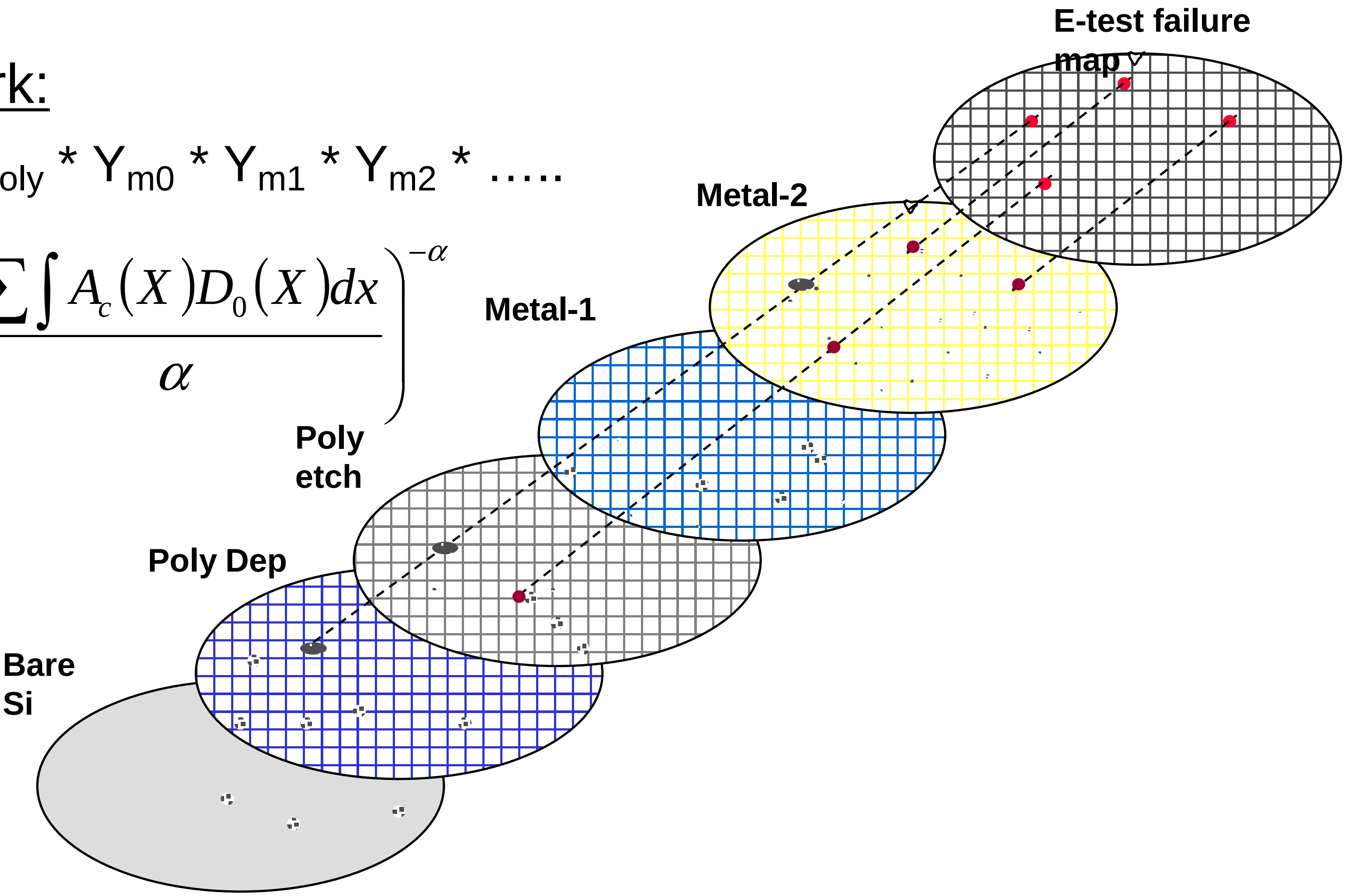
Micro-Yield Model

Process level physical defects → (Test structure) Yield

<u>This work:</u>

$$Y_R = Y_{poly} * Y_{m0} * Y_{m1} * Y_{m2} * \ldots..$$

$$Y_R = \left(1 + \frac{\sum \int A_c(X) D_0(X) dx}{\alpha}\right)^{-\alpha}$$



Key Changes in 2002 Electronic Update

- **For the Defect Detection & Characterization (DDC) section, table changes were made to either correct typing errors or make technology requirements consistent with the rest of the roadmap.**
- **For the Yield Learning (YL) section, table changes were made to reflect the following assumption changes:**
  - **The inspection sampling rate during yield ramp was changed from 20% to 10%**
  - **The cycle time per mask level was changed from 1 day to 1.5 days**
  - **Time to source new yield detractors was changed from 0.5X cycle time to 1X cycle time**
  - **Appearance of new defects/faults during yield ramp was changed from 1 per month to 4 per year**

Key Changes in 2002 Electronic Update continued

- **For the Yield Model and Defect Budget (YMDB) section, the ITWG members recommended using the <u>cluster coefficient of 2 instead of 5</u>. This revision will be made in 2003.**
- **For the Wafer Environment Contamination Control (WECC) section, besides clarifying the notes associated with the technology requirements table, the <u>particle size distribution for fluids/gases</u> of interest has been specified as <u>$f(x)=K*1/X^{2.2}$</u> based on a reference cited in the notes.**

Types of Models

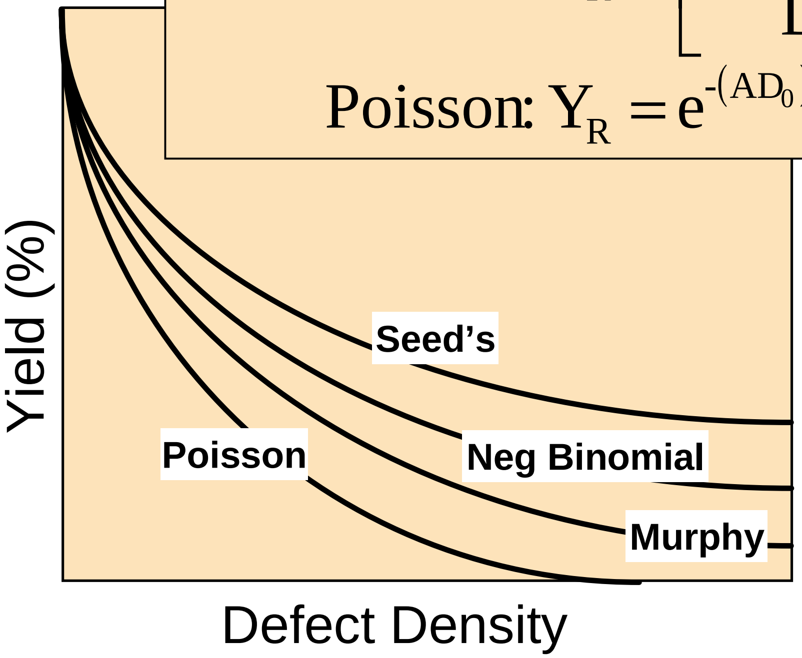
- Negative Binomial Model:
  - Large degree of clustering: $\alpha = 1$ (Seed’s)
  - Moderate clustering: $\alpha = 2$ (Neg Binomial)
  - Minor degree of clustering: $\alpha = 4.5$ (Murphy’s)
  - Lack of clustering: $\alpha > 7$ (Poisson)
- The “Negative Binomial” model provides greater flexibility for applications involving larger chip sizes, lower yield levels, defect clustering, and larger wafer sizes

Seed's: $Y_R = \frac{1}{(1+AD_0)}$

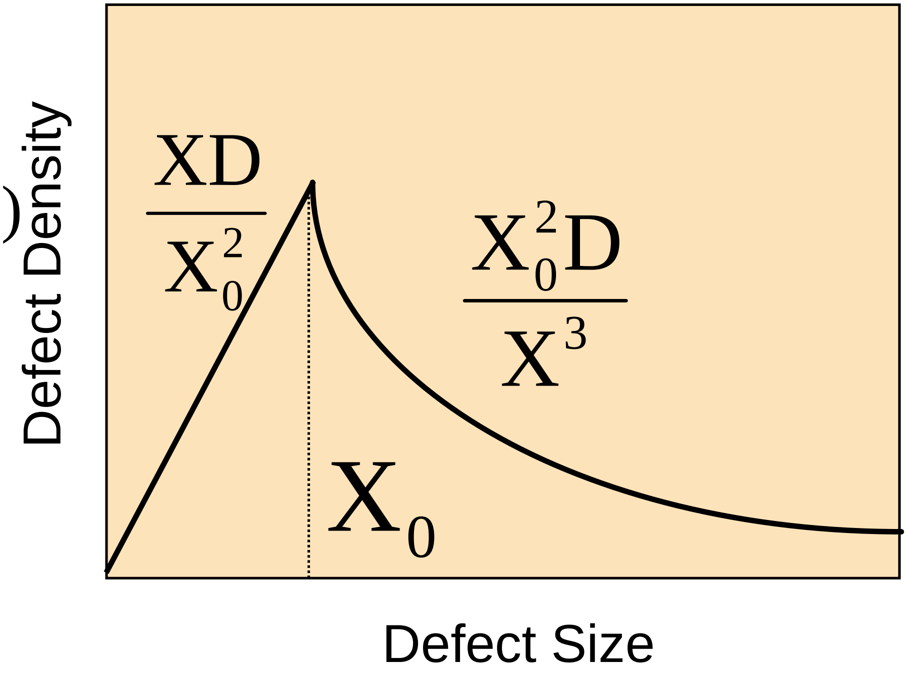
Neg Binomial: $Y_R = \left(1+\frac{(A_cD_0)}{\alpha}\right)^{-\alpha}$

Murphy's: $Y_R = \left[\frac{\left(1-e^{-(AD_0)}\right)}{D_0A}\right]^2$

Poisson: $Y_R = e^{-(AD_0)}$



Defect Size Distribution



- The $1/x^3$ defect size (differential) distribution has been widely demonstrated
- Provides the capability to predict (cumulative) defect densities at other defect sizes:

$$\frac{D_2}{D_1} = \left(\frac{X_1}{X_2}\right)^2$$

- If the exponent is less than "3", then the yields will improve with shrinking dimensions (results in fewer smaller particles)

Example of 2002 Update – Portion of Table 93a DDC Tech. Req. - Near-term

	Year of Production	2001	2002	2003	2004	2005	2006	2007	Driver
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	
Was	*Patterned Wafer Inspection, PSL* Spheres at 90% Capture, Equivalent Sensitivity (nm) [A, B]*								
Is									
Was	Process R&D at 300 cm^2/hr (1 wafer/hr)	**78**	**72**	**66**	**54**	**48**	**42**	**39**	*0.6 x DR*
Is	Process R&D at 300 cm^2/hr (1 wafer/hr)		🟨	🟨	🟨	🟨	🟨	🟨	
Was	Yield ramp at 1200 cm^2/hr (4 wafer/hr)	**104**	**96**	**88**	**72**	**65**	**56**	**52**	*0.8 x DR*
Is	Yield ramp at 1200 cm^2/hr (4 wafer/hr)	**104**	**96**	**88**	**72**	**64**	**56**	**52**	*0.8 x DR*
Was	Volume production at 3000 cm^2/hr (10 wafe	**130**	**120**	**110**	**90**	**80**	**70**	**66**	*1.0 x DR*
Is	Volume production at 3000 cm^2/hr (10 wafer/hr)			🟨	🟨	🟨	🟥	🟥	
Was	*High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[C]*								
Is									
Was	All stages of manufacturing	**130**	**120**	**110**	**90**	**80**	**70**	**65**	*1.0 x DR*
Is	All stages of manufacturing	🟨	🟨	🟨	🟥	🟥	🟥	🟥	
Was	Process verification (1 wafer/hr)	**130**	**120**	**110**	**90**	**80**	**70**	**65**	*1.0 x DR*
Is	Process verification (1 wafer/hr)	🟨	🟨	🟨	🟥	🟥	🟥	🟥	
Was	Volume manufacturing (4 wafer/hr)	**130**	**120**	**110**	**90**	**80**	**70**	**65**	*1.0 x DR*
Is	Volume manufacturing (4 wafer/hr)	🟥	🟥	🟥	🟥	🟥	🟥	🟥	
Was	Cost of Ownership :volume manufacturing, non-HARI ($/wafer scanned, 10/hr)	**2–5**	**2–5**	**2–5**	**3–7**	**3–7**	**3–7**	**3–7**	
Is	Cost of Ownership :volume manufacturing, non-HARI ($/wafer scanned, 10/hr)				🟨	🟨	🟨	🟨	
Was	CoO HARI	**20–50**	**20–50**	**20–50**	**20–50**	**20–50**	**20–50**	**20–50**	
Is	CoO HARI	🟥	🟥	🟥	🟥	🟥	🟥	🟥	

Example of 2002 Update - Table 94a YL Tech. Req. - Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Was	*Wafer size (mm)*	**300**	**300**	**300**	**300**	**300**	**300**	**300**
Is	*Wafer size (mm)*	**300**	**300**	**300**	**300**	**300**	**300**	**300**
Was	*Number of mask levels*	**25**	**25**	**25**	**27**	**27**	**27**	**29**
Is	*Number of mask levels (simple logic)*	**25**	**25**	**25**	**27**	**27**	**27**	**29**
Was	*Number of processing steps (simple logic)*	**490**	**503**	**516**	**530**	**543**	**556**	**570**
Is	*Number of processing steps*	**490**	**503**	**516**	**530**	**543**	**556**	**570**
Was	*Cycle time during ramp (# days)*	**25**	**25**	**25**	**27**	**27**	**27**	**29**
Is	*Cycle time during ramp (# days)*	**38**	**38**	**38**	**41**	**41**	**41**	**44**
Was	*Defect/Fault Sourcing Complexity [A], [G]*							
Is	*Defect/Fault Sourcing Complexity [A], [G]*							
Was	Logic transistor density/cm^2 (1E6)	**14**	**19**	**26**	**35**	**47**	**63**	**85**
Is	Logic transistor density/cm^2 (1E6)	**14**	**19**	**26**	**35**	**47**	**63**	**85**
Was	Defect sourcing complexity factor (1E9) [B]	**7**	**10**	**13**	**18**	**25**	**35**	**49**
Is	Defect sourcing complexity factor (1E9) [B]	**7**	**10**	**13**	**18**	**25**	**35**	**49**
Was	Defect sourcing complexity trend [C]	**1**	**1**	**2**	**3**	**4**	**5**	**7**
Is	Defect sourcing complexity trend [C]	**1**	**1**	**2**	**3**	**4**	**5**	**7**
Was	*Data Analysis for Rapid Defect/Fault Sourcing*							
Is	*Data Analysis for Rapid Defect/Fault Sourcing*							
Was	Patterned wafer inspection sensitivity (nm) during yield ramp	**104**	**96**	**88**	**72**	**64**	**56**	**52**
Is	Patterned wafer inspection sensitivity (nm) during yield ramp	**104**	**96**	**88**	**72**	**64**	**56**	**52**
Was	Average # of inspections/wafer during full flow	**5**	**5**	**5**	**5.4**	**5.4**	**5.4**	**5.8**

Table 94a YL Tech. Req. - Near-term…continued

Is	Average # of inspections/wafer during full flow	2.5	2.5	2.5	2.7	2.7	2.7	2.9
Was	Defect data volume (DV) (# data items/wafer) (1E13) [D]	5.5	7.1	9.4	12.5	15.8	20.7	25.7
Is	Defect data volume (DV) (# data items/wafer) (1E13) [D]	2.75	3.55	4.7	6.25	7.9	10.35	12.85
Was	Defect data volume (DV) trend [E]	1	1	2	2	3	4	5
Is	Defect data volume (DV) trend [E]	1	1	2	2	3	4	5
Was	*Yield Learning During Ramp from 30% to 80% Sort Yield [F]*							
Is	*Yield Learning During Ramp from 30% to 80% Sort Yield [F]*							
Was	# of yield learning cycles/year based on full flow cycle time	14.6	14.6	14.6	13.5	13.5	13.5	12.6
Is	# of yield learning cycles/year based on full flow cycle time	9.7	9.7	9.7	9.0	9.0	9.0	8.4
Was	Required yield improvement rate per learning cycle	3.4	3.4	3.4	3.7	3.7	3.7	4
Is	Required yield improvement rate per learning cycle	5.1	5.1	5.1	5.5	5.5	5.5	6.0
Was	Time to identify and fix new defect/fault source during ramp	12.5	12.5	12.5	13.5	13.5	13.5	14.5
Is	Time to identify and fix new defect/fault source during ramp	38	38	38	41	41	41	44
Was	# of learning cycles/year for 1 defect/fault sources/month	8.6	8.6	8.6	7.5	7.5	7.5	6.6
Is	# of learning cycles/year for 4 defect/fault source/year	5.7	5.7	5.7	5.0	5.0	5.0	4.4
Was	Required yield improvement rate/learning cycle for 1 defect/fault source/month	5.8	5.8	5.8	6.7	6.7	6.7	7.6
Is	Required yield improvement rate/learning cycle for 4 defect/fault sources/year	8.7	8.7	8.7	10.0	10.0	10.0	11.4
Was	***Excursion Control***							
Is	***Excursion Control***							
Was	Time to recognize defect trend $T_{RT} = f(T_{MP}, N, T_C, V)$ [H]	*	*	*	*	*	*	*
Is	Time to recognize defect trend $T_{RT} = f(T_{MP}, N, T_C, V)$ [H]	*	*	*	*	*	*	*
Was	Time to recognize electrical fault signature	*	*	*	*	*	*	*
Is	Time to recognize electrical fault signature	*	*	*	*	*	*	*
Was	Time to identify defect mechanism $T_{ID} = f(T_{RT}, N, M, R)$ [H]	*	*	*	*	*	*	*
Is	Time to identify defect mechanism $T_{ID} = f(T_{RT}, N, M, R)$ [H]	*	*	*	*	*	*	*

Changes and Additions for 2003

- **Limit scope to wafer sort yield.**
- **Look at the relationship between yield enhancement and manufacturing process control. Also connect the yield learning section to other TWGs.**
- Add new difficult challenges and new topics:
  - **Line edge roughness, ACLV, subtle process variation**
  - **Where does process variation stop and defect start?**
  - **Contamination transferred from wafer edge and backside**
  - **Unified definition of defects based on yield impact**
- **Must come up with creative solutions to improve yield learning rate because of increasing complexity and cycle time.**
- **Expand on new material coverage extending classical CMOS (i.e. high κ, Low κ, and Cu in all 4 focus topics).**
- **Drive the roadmap based on 300mm wafer size and issues critical to making high yielding 300mm fabs.**
- **Include commonality and uniqueness beyond classical CMOS i.e. SOI, SiGe, strained silicon, etc. in all 4 focus topics (DDC, YL, YMDB, WECC).**

Overall future challenges

Key challenges

-high aspect ratio inspection and review possibility

-Integration of in-line physical failure analysis to improve root cause identification

- signal/noise : sorting of defects of interest vs nuisance defects
- cycle time / yield learning challenges

Cross functional challenges with design subgroup

- design for yield
  automation for recommended rules, implementation of DFM in productive environment (tools). For e.g. minimize critical area, add redundant rows, columns & vias and metal extensions.
- design for test/analysis

Other challenges

- structural test (bitfail map with pattern recognition for logic), procedures to extract fault densities
- non visual defect source
- cost of yield
- yield vs throughput (production needs limit useable sensitivity)

Summary

- **Four of five regions around the world are now actively participating in the Yield Enhancement roadmap development activity.**
- **The 2002 electronic update has minor changes in 3 of 4 sections. However, several assumptions were changed for the Yield Learning section further highlighting rapid yield ramp as a major challenge.**
- **Defect detection in high aspect ratio structures continues to be a grand challenge.**
- **We have begun the brainstorming process for 2003 revision with numerous suggestions for improvements received to date.**