2002 ITRS Test Chapter Update

ITRS Test ITWG

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Test ITWG Membership

- Japan
  - ATE Sub-WG
  - DFT Sub-WG
- Europe
  - Agilent
  - Infineon
  - Philips
  - ST Microelectronics
- US
  - Advantest
  - Agere
  - IBM
  - Inovys
  - Intel
  - NPTest
  - Synopsys
  - Teradyne
  - Texas Instruments

Participation from Taiwan and Korea regions needed!

2002 ITRS Test Chapter Update

- Trends described in 2001 have held true
  - High speed interfaces are appearing in a broad range of applications in many market segments
  - SOC and SIP dominate new designs
  - Low cost, targeted test platforms emerging

The 2002 update will bring only minor adjustments to the trends defined in 2001

2001 Key Challenges

- High Speed Device Interfaces
- Highly Integrated Designs & SOCs
- Reliability Screens
- Manufacturing Test Cost Reduction
- Standards
- Test Environment Modeling and Simulation

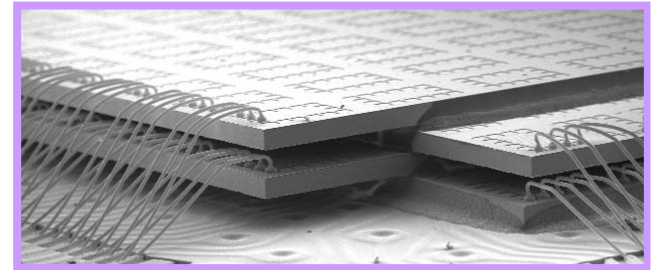
Interim solutions have emerged, however new technology development continues to outpace the test equipment design cycle

Demand for Bandwidth

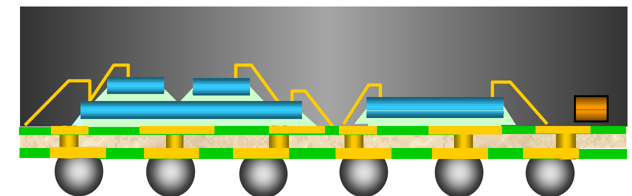
- Learning rate for cost effective manufacturing ATE solutions lags leading edge device technology
  - Capability at the high end (10G, 40G)
  - Integration level at the low end (3G)
- DFT-based test methods in development to provide low cost manufacturing test for high integration devices
  - Unclear if complete device validation can be provided with DFT
- Protocol complexity of high speed bus interfaces is outpacing functional tester capability
  - Concept of "soft" testers

Year of Production		*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
MPU / ASIC ½ Pitch (nm)		*150*	*130*	*107*	*90*	*80*	*70*	*65*
High-integration-level backplane and computer I/O								
Serial data rate (Gbits/s)	Production	**2.5**	**3.125**	**3.125**	**10**	**10**	**40**	**40**
	Introduction	**3.125**	**—**	**10**	**—**	**40**	**—**	**—**
Maximum port count	at Production frequencies	**20**	**100**	**200**	**100**	**200**	**100**	**200**
	at Introduction frequencies	**—**	**—**	**20**	**—**	**20**	**—**	**—**

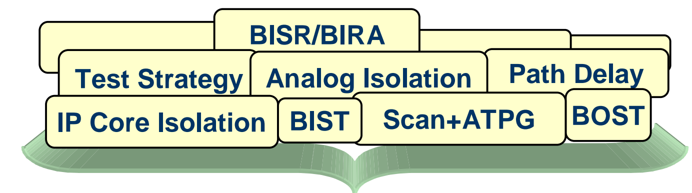
High Integration Devices & SOC

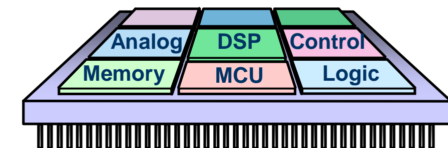


- Customer requirements for form factor and power consumption are driving a significant increase in design integration levels
  - Test complexity will increase dramatically with the combination of different classes of circuits on single die or within a single package
  - Disciplined, structured DFT is a requirement to reduce test complexity – test packaged with IP



- New test methods and equipment architectures must be developed
  - Potential for DFT on one die to address testability issues for another
  - Enable a merge of logic and analog test capability with the throughput of high density memory test equipment





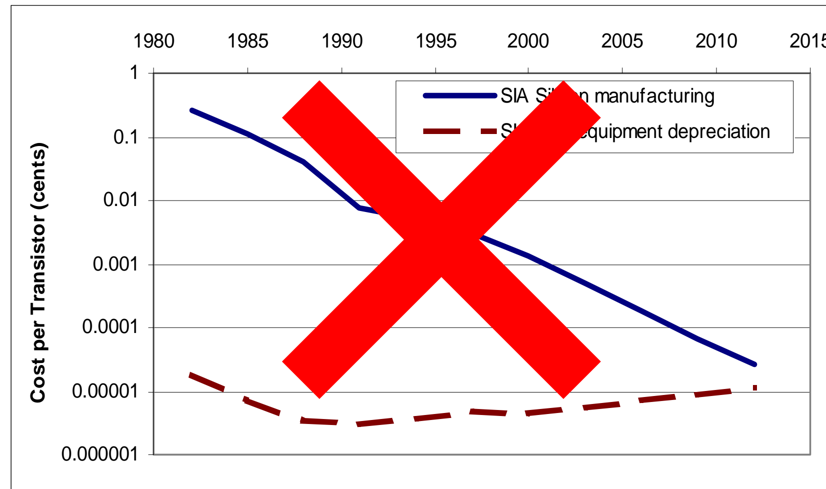
IP Core Based Design

Running Out of Gas

- Reliability screens
  - Burn-in methods limited by thermal runaway
  - Lowered use voltages limits voltage stress opportunity
  - Difficulty of determining Iddq signal versus “normal” leakage current noise

- Physical techniques for diagnosis and failure analysis
  - Active circuit probing limited by small transition energies
  - Circuit edit (FIB) limited by shrinking dimensions

The Industry is Changing



- Efforts to increase production module throughput and reduce test equipment capability requirements - cost has begun to scale
  - Growing divergence between capability expectation of characterization versus manufacturing equipment
- Test cost as a percentage of overall product cost remains high for many products
  - Test cost is based on device function, not fab process or die size
  - >30% of manufacturing cost for some products

Dismantling the Red Brick Walls

- Design For Test enabling has begun to remove many of the roadblocks that appeared in the 1997 and 1999 roadmaps
  - Test is becoming integrated with the design process
  - Improvements demonstrated in capability and cost
  - More prevalent in IDM than Foundry
- Continued research is needed into new and existing digital logic fault models
  - Identification of true process defects
  - Anticipation of potential defects in new process steps
- Development of Analog DFT methods must advance
  - Formalization of analog techniques and development of fault models

The Consequence of Low Cost

- Targeted, low cost test platforms have positive cost impact for the products they serve
- However… they dramatically increase capacity management complexity
  - In the extreme this could be a tester per product or product family
  - Effective utilization of a diverse manufacturing fleet presents a significant challenge
  - In the end overall manufacturing cost impact may be negative
- A new paradigm is needed to achieve low cost without dramatic increase in the diversity of platforms
  - Open Architectures emerging from supply base

Standards Focus

- Standards for test equipment interface & communication are needed to decrease equipment factory integration time
  – Improve equipment interoperability to reduce factory systems integration time
- Standards for ATE software and test program generation are needed to decrease test development effort and improve time to market
  – Lower the barrier for selecting the optimal equipment
- Increased focus for standards development and adoption of existing standards
  – Mechanical docking and interface standards
  – Data transfer from Fab to Wafer Probe to Assembly to Component Test to Finish

Roadmap Directions

- Minor updates to trends in 2002
- 2003 effort focused on:
  - Reliability Methods
  - Device Interface
  - Material Handling
  - Wafer Parametric Test
  - 2001 Key Challenges

  - Increased international participation
    - Japan, Europe, and US well represented
    - Need engagement from Taiwan and Korea regions