

The 2002 ITRS

Assembly and Packaging Roadmap

Joe Adam TWIG Co-chair



International Technology Roadmap for Semiconductors

4 December 2002, ITRS 2002 Update Conference

Key ITRS Contributors

Ryo Haruta – Hitachi
Kazuto Tsuji – Fujitsu
Yuji Shirai – ASET
Shoji Uegaki – Kyocera
Kuniaki Takahashi – Toshiba
Hisao Kasuga – NEC
Raymond Saito - Ihara
Mark Bird - Amkor
Bill Bottoms - 3MTS
Ted Zarbuck - Intel
Chi Shih Chang - HCD
Bill Chen - ASE

Ed Fulcher - LSI
Mahadevan Iyer - IME
Bernd Roemer - IFX
Henry Utsunomiya - Jisso
Jurgen Wolf – IZM
Joe Adam – Skyworks
Tsungyao Chu – TSMC
Wen Kun Yang – ASE
Ted Ho – ITRI
Chen-Der Huang – TSMC
Lewis Hwan – Chipbond



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Changes To The 2002 Requirements Tables

- **Cost per pin numbers have adjusted down across all segments**
 - No Known solutions for many out year targets
 - Cost targets still put the cost of packaging well above cost of die
- **Pin counts have been adjusted down in the near term**
 - Pin counts still drive wiring density in packages very aggressively
- **Power will continue to increase in the high end and related frequency for I/O has been increased to include new communications requirements**
- **I/O pitches for wirebond increased near term**
- **Flip Chip chip pitches increased near term**
- **BGA pitches have been reduced**
- **Substrate line width and density reduced**



Packaging Near Term Requirements

Was	Low Cost	0.30–0.75	0.28–0.68	0.26–0.62	0.25–0.56	0.24–0.51	0.23–0.46	0.22–0.41
Is	Low Cost, Hand held and Memory The color applies to the low end only and are due only to cost. The high end numbers are OK	0.30–0.75	<u>0.30–0.62</u>	<u>0.30–0.56</u>	Scale @ 5% per year			
Was	Hand-held	0.45–0.90	0.42–0.81	0.40–0.73	0.38–0.65	0.36–0.60	0.34–0.56	0.32–0.52
Is	Hand-held Delete these categories	0.45–0.90	<u>0.30–0.62</u>	<u>0.30–0.56</u>	Scale @ 5% per year			
Was	Cost-performance	0.80–1.60	0.75–1.44	0.70–1.30	0.66–1.17	0.61–1.06	0.56–1.03	0.53–1.00
Is	Cost-performance	0.80–1.60	<u>0.75–1.30</u>	<u>Scale @ 5% per year high end keep low end due to added complexity (power, pad pitch, increased bumps per die, etc)</u>				
	High-performance	2.2	2.09	1.98	1.88	1.78	1.69	1.61
Was	Harsh	0.45–4.00	0.40–3.60	0.36–3.20	0.32–2.88	0.29–2.59	0.26–2.33	0.23–2.11
Is	Harsh Pb free will cause consolidation with other categories	0.45–4.00	0.40–3.60	0.36–3.20	0.32–2.88	0.29–2.59	0.26–2.33	0.23–2.11
Was	Memory	0.36–1.54	0.34–1.39	0.32–1.26	0.30–1.14	0.28–1.03	0.27–0.93	0.27–0.84
Is	Memory Delete these categories	0.36–1.54	0.34–1.39	0.32–1.26	<u>0.30–1.14</u>	<u>0.28–1.03</u>	<u>0.27–0.93</u>	<u>0.27–0.84</u>



Wirebond and Flip Chip Pitches

Table 77 Chip to Next Level Potential Solutions

Year of Production		2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65	45	32	22
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65	50	35	25
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35	25	18	13
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25	18	13	9
Chip Interconnect Pitch (µm)											
Was	Wire bond—ball	45	35	30	25	20	20	20	20	20	20
Is	Wire bond—ball	45	<u>40</u>	<u>35</u>	<u>30</u>	<u>25</u>	20	20	20	20	20
Was	Wire bond—wedge	40	35	30	25	20	20	20	20	20	20
Is	Wire bond—wedge	<u>50</u>	<u>50</u>	<u>40</u>	<u>40</u>	<u>35</u>	<u>35</u>	<u>30</u>	20	20	20
Was	TAB*	40	40	40	40	30	30	30	30	30	30
Is	TAB* Japan TWG has the lead for Tab technologies	<u>45</u>	40	<u>35</u>	<u>35</u>	30	30	<u>25</u>	<u>20</u>	<u>20</u>	<u>15</u>
Was	Flip chip (area array for cost-performance and high-performance)	160	160	150	150	130	130	120	90	80	70
Is	Flip chip area array	<u>200</u>	<u>180</u>	150	150	<u>100</u>	<u>100</u>	<u>80</u>	<u>70</u>	<u>70</u>	<u>50</u>
Was	Peripheral flip chip for hand-held, low-cost, and harsh	150	130	120	110	100	90	80	60	45	30
Is	Peripheral flip chip	<u>80</u>	<u>80</u>	<u>60</u>	<u>60</u>	<u>40</u>	<u>40</u>	<u>30</u>	<u>20</u>	<u>20</u>	<u>15</u>



BGA I/O pitches

Table 78 Ball Grid Array Packages Potential Solutions

Year of Production		2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM ½ Pitch (nm)		130	115	100	90	80	70	65	45	32	22
MPU / ASIC ½ Pitch (nm)		150	130	107	90	80	70	65	50	35	25
MPU Printed Gate Length (nm)		90	75	65	53	45	40	35	25	18	13
MPU Physical Gate Length (nm)		65	53	45	37	32	28	25	18	13	9
<i>BGA Solder Ball Pitch (mm)</i>											
Was	Low cost	1	1	0.8	0.8	0.65	0.65	0.65	0.5	0.5	0.5
Is	Low cost	1	<u>0.8</u>	0.8	0.8	<u>0.5</u>	<u>0.5</u>	<u>0.5</u>	0.5	0.5	0.5
Was	Hand-Held	1	1	0.8	0.8	0.65	0.65	0.65	0.5	0.5	0.5
Is	Hand-Held	1	<u>0.8</u>	0.8	0.8	<u>0.5</u>	<u>0.5</u>	<u>0.5</u>	0.5	0.5	0.5
Was	Cost-performance	1	1	0.8	0.8	0.65	0.65	0.65	0.5	0.5	0.5
Is	Cost-performance	1	1	<u>1</u>	0.8	<u>0.8</u>	<u>0.8</u>	<u>0.5</u>	0.5	0.5	0.5
Was	High-Performance	0.8	0.8	0.8	0.8	0.65	0.65	0.65	0.5	0.5	0.5
Is	High-Performance	0.8	<u>1</u>	<u>1</u>	<u>1</u>	<u>1</u>	<u>0.8</u>	<u>0.8</u>	<u>0.8</u>	<u>0.8</u>	<u>0.8</u>
Was	Harsh	1.27	1.27	1	1	1	0.8	0.65	0.5	0.5	0.5
Is	Harsh	1.27	1.27	1	1	1	0.8	<u>0.8</u>	0.5	0.5	0.5



Substrate Technology

Table 80 BGA and FBGA/CSP Package Substrate Potential Solutions

Year of Production	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65	45	32	22
MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65	50	35	25
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35	25	18	13
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25	18	13	9
Was FBGA/CSP solder ball pad pitch (mm)	0.4	0.4	0.4	0.4	0.3	0.3	0.3	0.3	0.3	0.25
Is FBGA/CSP solder ball pad pitch (mm)	<u>0.5</u>	<u>0.5</u>	0.4	0.4	0.3	0.3	<u>0.2</u>	<u>0.15</u>	<u>0.15</u>	<u>0.1</u>
Was Pad size (µm)	160	160	160	160	120	120	120	120	120	100
Is Pad size (µm)	<u>200</u>	<u>200</u>	160	160	120	120	120	120	120	100
Was Line width (µm)	48	48	48	48	36	36	36	36	36	30
Is Line width (µm)	<u>60</u>	<u>60</u>	48	48	36	36	<u>24</u>	<u>18</u>	<u>18</u>	<u>12</u>
Was Line spacing (µm)	48	48	48	48	36	36	36	36	36	30
Is Line spacing (µm)	<u>60</u>	<u>60</u>	48	48	36	36	<u>24</u>	<u>18</u>	<u>18</u>	<u>12</u>
# Rows accessed	3	3	3	3	3	3	3	3	3	3



2003 Roadmap Development

- Tables updates
 - Review on cost, pin count, frequency, pitches
- Major effort on the market sectors
- New tables on emerging technologies
 - MEMS device roadmap
 - Optoelectronics
 - Embedded components
 - System in a Package
 - Materials
 - Substrate technologies
- New sections on emerging technologies
 - Design, modeling, and simulation
 - ESD
 - High frequency
 - Implantable



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