

PIDS Key Issues for 2002 and 2003

ITRS

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International Technology Roadmap for Semiconductors

4 December 2002, ITRS 2002 Update Conference

Outline

- **PIDS Scope**
- **2002 changes**
- **2003 key issues**
- **Emerging Research Devices directions for 2003**
- **Summary**



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PIDS Scope

- **PIDS = Process Integration, Developments, and Structures**
- **Deals with**
 - Process integration and full process flows
 - MOSFET and passive devices and structures
 - Device physical and electrical characteristics and requirements
 - Reliability
- **Subcategories**
 - Memory and logic
 - Mixed-signal devices
 - Reliability
 - Also includes Emerging Research Devices Section (new in 2001 ITRS)



Changes in 2002 PIDS Chapter

- **Low Standby Power (LSTP) technology requirements: physical gate length scaling is slowed by one year compared to 2001 ITRS (see dark boxes, next few slides)**
 - As a result, performance and power dissipation scaling are slowed
 - This more accurately reflects real LSTP technology scaling
- **Other changes are relatively minor**
 - Updates
 - Clearer explanations in the notes and wording
- **Major changes, issues will be dealt with in 2003 ITRS**



LSTP Changes for 2002: Near-term

Table 36c Low Standby Power (LSTP) Technology Requirements—Near-term

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Was Physical gate length low-standby power (LSTP) (nm) [1]	90	75	65	53	45	37	32
Is Physical gate length low-standby power (LSTP) (nm) [1]	100	90	75	65	53	45	37
Was Equivalent physical oxide thickness for LSTP (EOT) (nm) [2]	2.4–2.8	2.2–2.6	2.0–2.4	1.8–2.2	1.6–2.0	1.4–1.8	1.2–1.6
Is Equivalent physical oxide thickness for LSTP (EOT) (nm) [2]							
Was Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.8	0.8	0.8	0.8	0.8	0.8	0.5
Is Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]							
Was T_{ox} electrical equivalent (nm) [4]	3.4	3.2	3	2.8	2.6	2.4	1.9
Is T_{ox} electrical equivalent (nm) [4]							
Was Nominal LSTP power supply voltage (V) [5]	1.2	1.2	1.2	1.2	1.2	1.2	1.1
Is Nominal LSTP power supply voltage (V) [5]							
Was Nominal LSTP NMOS sub-threshold current ($\alpha^2 \mathcal{E}$) (pA/ μ^2 m) [6]	1	1	1	1	1	1	1
Is Nominal LSTP NMOS sub-threshold current ($\alpha^2 \mathcal{E}$) (pA/ μ^2 m) [6]							
Was Nominal LSTP NMOS saturation current drive I_{sat} (at V_{dd} , at 25°C) (mA/ μ^2 m) [7]	300	300	400	400	400	400	500
Is Nominal LSTP NMOS saturation current drive I_{sat} (at V_{dd} , at 25°C) (mA/ μ^2 m) [7]							
Was Required percent current-drive "mobility/transconductance improvement" [8]	0%	0%	0%	0%	0%	0%	0%
Is Required percent current-drive "mobility/transconductance improvement" [8]							
Was LSTP NMOS device C_{gate}^2 ($C_{gate} * V_{dd} / I_{d-NMOS}$) (ps) [9]	4.61	4.41	2.96	2.68	2.51	2.32	1.81
Is LSTP NMOS device C_{gate}^2 ($C_{gate} * V_{dd} / I_{d-NMOS}$) (ps) [9]	5.02	4.84	3.31	3.12	2.83	2.66	2.01
Was LSTP relative device performance [10]	1	1.05	1.6	1.7	1.8	2	2.6
Is LSTP relative device performance [10]	1	1.04	1.52	1.61	1.77	1.89	2.50
Was Energy per ($W/L_{gate}=3$) device switching transition $\frac{1}{2} C_{gate} * (3 * L_{gate}) * V^2$ (fJ/device) [11]	0.448	0.381	0.277	0.204	0.163	0.123	0.095
Is Energy per ($W/L_{gate}=3$) device switching transition $\frac{1}{2} C_{gate} * (3 * L_{gate}) * V^2$ (fJ/device) [11]	0.542	0.471	0.357	0.292	0.216	0.172	0.122
Was Static power dissipation per ($W/L_{gate}=3$) device (Watts/device) [12]	3.20E-13	2.90E-13	2.30E-13	1.90E-13	1.60E-13	1.30E-13	1.10E-13
Is Static power dissipation per ($W/L_{gate}=3$) device (Watts/device) [12]	3.60E-13	3.24E-13	2.70E-13	2.34E-13	1.91E-13	1.62E-13	1.22E-13



LSTP Table Changes for 2002: Long-Term

Table 36d Low Standby Power (LSTP) Technology Requirements—Long-term

Year of Production	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU / ASIC ½ Pitch (nm)	50	35	25
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Was Physical gate length low-standby power (LSTP) (nm) [1]	22	16	11
Is Physical gate length low-standby power (LSTP) (nm) [1]	28	20	16
Was Equivalent physical oxide thickness for LSTP T_{ox} (EOT) (nm) [2]	0.9-1.3	0.8-1.2	0.7-1.1
Is Equivalent physical oxide thickness for LSTP T_{ox} (EOT) (nm) [2]			
Was Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.5	0.5	0.5
Is Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]			
Was T_{ox} electrical equivalent (nm) [4]	1.6	1.5	1.4
Is T_{ox} electrical equivalent (nm) [4]			
Was Nominal LSTP power supply voltage (V_{dd}) (V) [5]	1	0.9	0.9
Is Nominal LSTP power supply voltage (V_{dd}) (V) [5]			
Was Nominal LSTP NMOS sub-threshold current (at 25 ° C) (pA/μm) [6]	3	7	10
Is Nominal LSTP NMOS sub-threshold current (at 25 ° C) (pA/μm) [6]			
Was Nominal LSTP NMOS saturation current drive (I_{dd}) (at V_{dd} , at 25° C) (μA/μm) [7]	500	600	700
Is Nominal LSTP NMOS saturation current drive (I_{dd}) (at V_{dd} , at 25° C) (μA/μm) [7]			
Was Required percent current-drive "mobility/transconductance improvement" [8]	10%	30%	50%
Is Required percent current-drive "mobility/transconductance improvement" [8]			
Was LSTP NMOS device τ ($C_{gate} * V_{dd} / I_{d-NMOS}$) (ps) [9]	1.43	0.91	0.66
Is LSTP NMOS device τ ($C_{gate} * V_{dd} / I_{d-NMOS}$) (ps) [9]	1.69	1.05	0.82
Was LSTP relative device performance [10]	3.2	5.1	7
Is LSTP relative device performance [10]	2.97	4.78	6.15
Was Energy per ($W/L_{gate}=3$) device switching transition ($C_{gate}*(3*L_{gate})*V^2$) (fJ/device) [11]	0.047	0.024	0.014
Is Energy per ($W/L_{gate}=3$) device switching transition ($C_{gate}*(3*L_{gate})*V^2$) (fJ/device) [11]	0.071	0.034	0.025
Was Static power dissipation per ($W/L_{gate}=3$) device (Watts/device) [12]	2.00E-13	3.00E-13	3.00E-13
Is Static power dissipation per ($W/L_{gate}=3$) device (Watts/device) [12]	2.52E-13	3.78E-13	4.32E-13



Key 2003 PIDS Issues

- **DRAM: re-evaluation of scaling – half pitch, EOT, cell size and cell size (“a”) factor, number of bits per chip, word line voltage**
 - Survey has been sent out: what is in production in 2002, plans beyond 2002
- **NVM (flash and FeRAM): changes in scaling of half pitch, cell size and cell size factor contemplated for 2003**
- **Reliability**
 - More detail on major failure mechanisms
 - Expand technology requirements
- **Logic**
 - Re-evaluation of scaling (assumptions, requirements and simplified models) for high-performance and low-power
 - Re-evaluation of maximum gate leakage current limit for high-performance logic
 - Add embedded SRAM roadmap



Key 2003 Cross-TWG Issues: Logic

- **With FEP TWG**
 - Parasitic $R_{s,d}$ modeling: PMOS and NMOS
 - Re-evaluation of maximum gate leakage current limits for high-performance logic
 - L_{eff} : process control requirements
 - Poly depletion requirements
 - SOI requirements
 - Begin to evaluate process and material requirements for non-classical CMOS
- **With Design**
 - Review of model-based scaling from a circuit point of view
 - Re-evaluation of maximum gate leakage current limits for high-performance logic
 - Evaluation of static power dissipation issues for high-performance logic
 - Use of multi- V_t , multi- T_{ox}
 - Circuit design, architecture power conditioning techniques
 - Dynamic or electrically alterable V_t



PIDS Emerging Research Devices Working Group: *Directions for 2003*

Technology Transfers

- ◆ Non classical CMOS (PIDS and FEP)
 - FDSOI (not including Ultra-Thin Body SOI with $t_{\text{si}} < 10$ nm)
 - Strained Si for enhanced channel mobility
- ◆ Memory (PIDS and FEP)
 - MRAM
 - Phase Change Memory
- ◆ Architecture (Assembly and Packaging)
 - 3D Integration using mechanical wafer attachment techniques

Technology Additions

- ◆ Capacitor-less DRAM cell
- ◆ Quantum memories
- ◆ Spintronics
- ◆ Silicon nanowires



PIDS Emerging Research Devices Working Group: ***Directions for 2003 (con't.)***

◆ **Add another node (15-nm node) to the 2003 Roadmap for CMOS?**

– **Silicon MOSFETs will operate for channel lengths down to 5 nm.**

– **IRC will determine node timing.**

◆ **Add new technology drivers to Mixed Signal in the 2003 ITRS to support wireless applications. Potential Solutions new to the ITRS include:**

– **Compound semiconductor technologies (GaAs and InP)**

– **MEMS Technologies**

◆ **Critically evaluate new Information Processing Technologies, based on application needs and technical criteria.**



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PIDS Summary

- **2002: minor updates and corrections**
- **2003: considerable re-evaluation, significant changes are contemplated**
- **Emerging research devices, 2003: some significant issues, changes, and additions**



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