

Modeling and Simulation ITWG

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4 December 2002, ITRS 2002 Update Conference

Key Messages

Update of key messages from 2001 ITRS:

- Technology modeling and simulation is one of a few enabling methodologies that can accelerate development times and reduce development costs: Assessment up to 25% in 2001, expected to increase
- Cross-cut links to the other ITRS sections were established - major goal of ITWG activities to further extend these links
- Accurate technology experimental characterization is essential
- Modeling and simulation provides an ‘embodiment of knowledge and understanding’. It is a tool for technology/device optimization and also for training/education



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Technology Modeling SCOPE & SCALES

Equipment related

- Equipment/feature scale
- Lithography

(Chapter sub-sections in blue)



Feature scale

- Front End, Back End
- Device

IC-scale

- Circuit elements
- Package modeling
- Interconnect performance modeling

- Materials Modeling
- Numerical Methods



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Key Messages (con't)

Trends / changes from 1999/2000 edition of ITRS

- Increased need for fundamental materials modeling and relating those results to electronic properties (e.g. gate stack)
- Need much better techniques / methodologies for exploring “end of the roadmap” issues.
- Stronger need for RF simulation methodologies.
- Need greater tie between models and chip design methodologies
- Need better analytical and characterization techniques to aid in the development of predictive models.
- Relevance of advanced numerical methods and algorithms increasing & more detailed in roadmap



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Key Messages (con't)

Trends / changes from 2001 edition of ITRS

- New long-term challenge “Compact modeling including more physical models and statistics”
- Two long-term challenges extended in scope
- Adapt “summary of issues” in challenges list to current technical progress and update of requirements (e.g. skip 248 nm)
- Details of near-term requirements adapted to current technical progress:
 - esp. lithography status and roadmap
 - esp. multi-level hierarchical simulation

ITWG actions in 2002

- Update 2001 tables
- Further increase interactions with other ITWGs & impact of simulation



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Difficult Challenges > 65 nm (I)

DIFFICULT CHALLENGES > 65 nm / THROUGH 2007	SUMMARY OF ISSUES
High frequency circuit modeling (>5 GHz)	<ul style="list-style-type: none"> • Efficient simulation of full-chip interconnect delay. • Accurate 3D interconnect model; inductance, transmission line models. • High frequency circuit models including non-quasi-static, substrate noise and coupling. • Parameter extraction without RF measurements .
Modeling of ultra shallow dopant distributions (junctions, activation) and silicidation	<ul style="list-style-type: none"> • Dopant models & parameters (damage, high-concentration, activation, metastable effects, diffusion, interface and silicide effects) in Si-based substrate, i.e. in Si, SiGe:C, (incl. strain), SOI and ultra-thin body devices. • Characterization tools for these ultra shallow geometries and dopant levels.
Modeling deposition and etch rate variations, feature geometry variations across a wafer	<ul style="list-style-type: none"> • Fundamental physical data (e.g. rate constants, cross sections, surface chemistry); reaction mechanisms and reduced models for complex chemistry. • Linked equipment / feature scale models. • CMP (full wafer and chip level, pattern dependent effects). • MOCVD, PECVD and ALD modeling • Multi-generation equipment/wafer models



Difficult Challenges > 65 nm (II)

DIFFICULT CHALLENGES > 65 nm / THROUGH 2007	SUMMARY OF ISSUES
Modeling of lithography technology	<ul style="list-style-type: none"> • Predictive resist models (incl. mechanical stability and etch resistance) • Line-edge roughness and its effect on circuit performance • Resolution enhancement techniques; mask synthesis (OPC, PSM). • 193 versus 157 evaluation and tradeoffs. • Multi--generation lithography system models
Gate stack models for ultra-thin dielectrics	<ul style="list-style-type: none"> • Electrical and process models for high-k gate dielectrics, metal gates, and alternative CMOS structures (Si-Ge, SOI and double gate) • Model dielectric constant, bulk polarization charge, surface states, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions

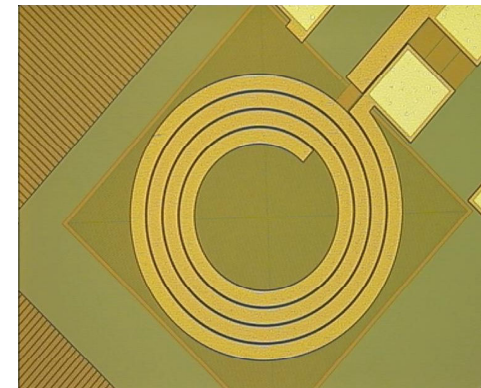
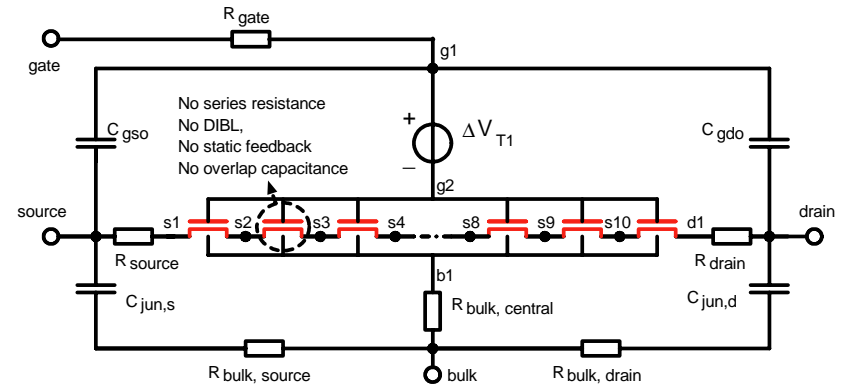


Difficult Challenges

High-Frequency Circuit Modeling (>5Ghz)

Needs

- Efficient simulation of full-chip interconnect delay
- Accurate 3D interconnect model; inductance, transmission line models
- High-frequency circuit models including
 - non-quasi-static effects
 - predictive noise behavior
 - coupling
- Reduction of high-frequency measurements needed for parameter extraction for active and passive devices



(From Philips)



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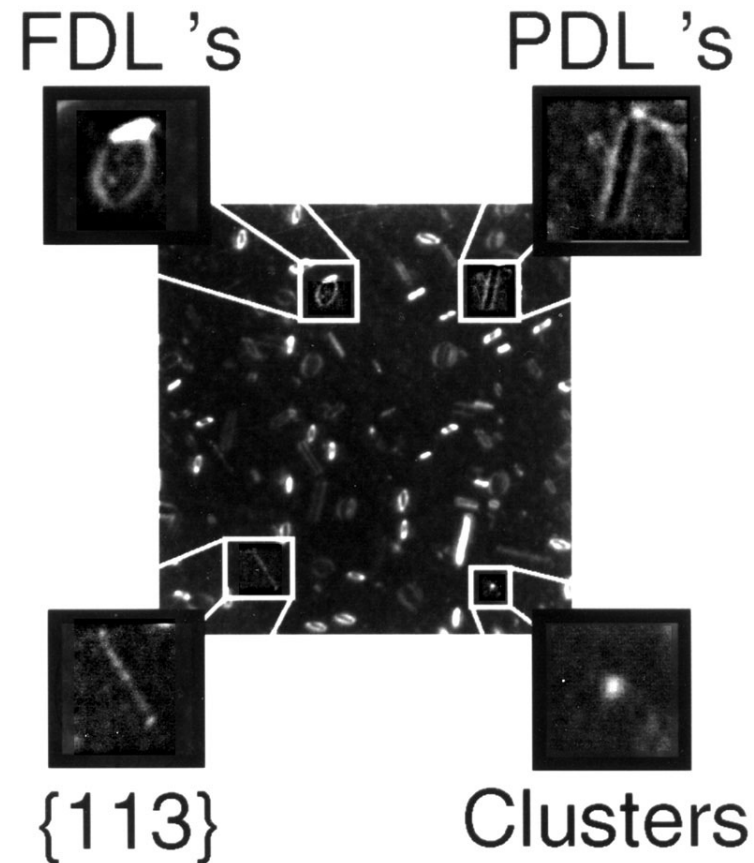
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Difficult Challenges

Modeling of Ultra Shallow Dopant Distributions (Junctions, Activation), and Silicidation

Needs

- Dopant models & parameters (damage, high-concentration, activation, metastable effects, diffusion, interface and silicide effects) in Si-based substrate, i.e. in Si, SiGe:C, (incl. strain), SOI and ultra-thin body devices
- Characterization tools for ultra-shallow geometries and dopant levels



Source: A. Claverie, CEMES/CNRS, Toulouse, France



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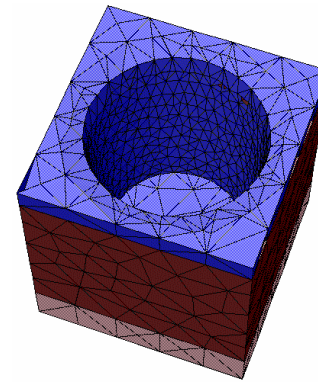
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Difficult Challenges

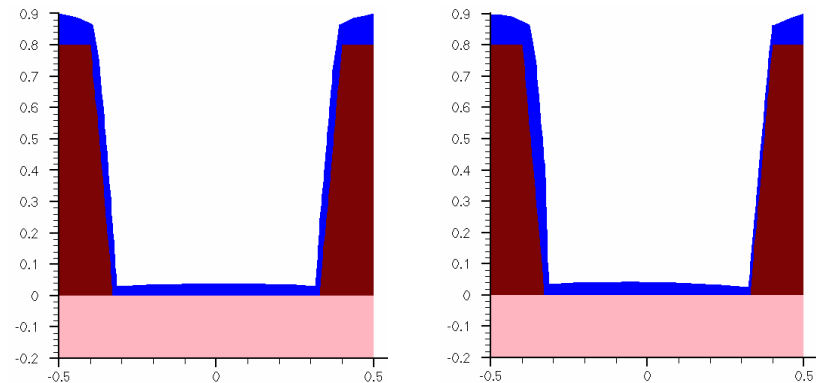
Modeling of Deposition and Etch Variations, and Feature Variations Across a Wafer

Needs

- Fundamental physical data (e.g. rate constants, cross sections, surface chemistry).
- Reaction mechanisms and reduced models for complex chemistries
- Linked equipment/feature scale models
- CMP (full wafer and chip level, pattern dependent effects)
- MOCVD, PECVD and ALD modeling
- Multi-generation equipment/wafer models



Simulated across-wafer variation of feature profile for a sputter-deposited barrier.



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Difficult Challenges

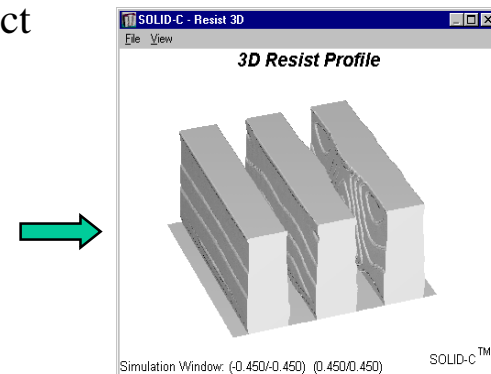
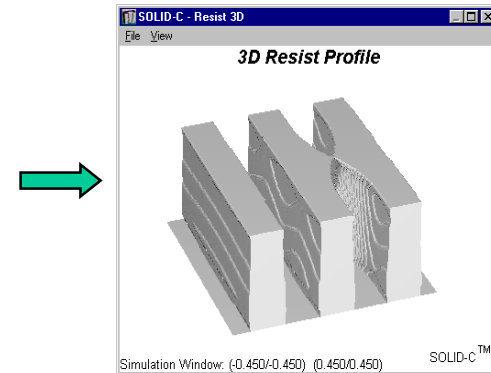
Modeling of Lithography Technology

Needs

- Predictive resist models (incl. mechanical stability and etch resistance)
- Line-edge roughness and its effect on circuit performance
- Resolution enhancement techniques; mask synthesis (OPC, PSM)
- 193 nm versus 157 nm evaluation and tradeoff methodologies.
- Multi-generation lithography system models



Printing of defect on phase-shift mask: bump defect (top) vs. etch defect (lower)



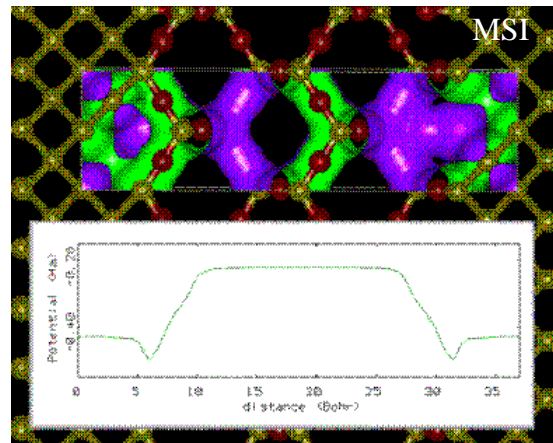
Difficult Challenges

Gate Stack Models for Ultra-thin Dielectrics

Needs

- Electrical and process models for high-k gate dielectrics, metal gates, and alternative CMOS structures (Si-Ge, SOI and double gate)
- Model dielectric constant, bulk polarization charge, surface states, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions

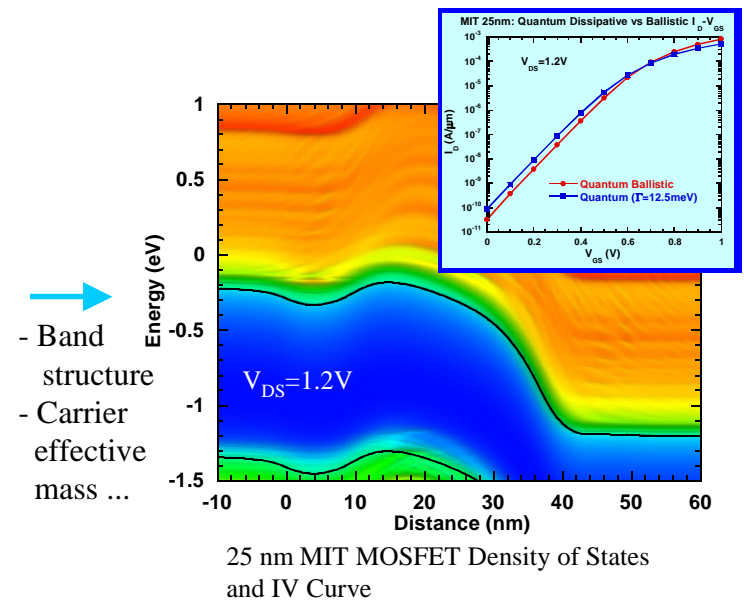
Use atomistic models to predict physical and electronic properties of materials; eg, HfO_2 .



Potentials in a thin SiO_2 layer.

Direct Applications

- Defect states
- Leakage current
- Impurity transport
- Processing recommendations ...



25 nm MIT MOSFET Density of States and IV Curve



Difficult Challenges < 65 nm

DIFFICULT CHALLENGES < 65 nm/ BEYOND 2007	SUMMARY OF ISSUES
Extend beyond continuum tools	A succession of modeling tools that combine atomistic effects with present day continuum software tools
Ultimate CMOS and nanoscale simulation capability	<ul style="list-style-type: none"> • Methods and algorithms which contribute to prediction of CMOS limits • Quantum based simulators • Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS • Models for device impact of statistical fluctuations in structures and dopant distributions
Compact modeling including more physical models and statistics	Computer-efficient inclusion of influences of statistics (incl. correlations) before process freeze, quantum/ballistic transport, etc. into compact modeling
Thermal-mechanical-electrical modeling for interconnections and packaging	<p>Model thermal- mechanical and electronic properties of Low-K, High-K and conductors and the impact of processing on these properties</p> <p>Model reliability of packages and interconnects, e.g. stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion</p>
Development and Seamless Integration of Software Modules incl. Advanced Algorithms	<ul style="list-style-type: none"> • Development of problem-specific algorithms • Seamless integration of simulation modules with focus on interplay and interfacing of the modules in order to enhance design effectiveness, metrology, by using design of experiment, job farming. Open / Standardized formats



Summary of New 2002 ITWG Recommendations

- Tables modified in details
- New long-term challenge “Compact Modeling Including Statistics”
- Two other long-term challenges broadened
- Long-term requirement for emerging devices: “Nanoscale simulation capability including accurate quantum models”
- Long-term requirement for Interconnect and Package Modeling - electrical/optical models: “Reliability prediction in coupled modeling”



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More details given on poster

Thank you



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