Metrology Roadmap
2002 Update

Europe	Ulrich Mantz (Infineon) Alec Reader (Philips Analytical) Mauro Vasconi (ST)
Japan	Masahiko Ikeno (Mitsubishi) Fumio Mizuno (Meisei University) Toshihiko Osada (Fujitsu) Akira Okamoto (SONY) Yuichiro Yamazaki (Toshiba)
Korea	DH Cho (Samsung)
Taiwan	Henry Ma (EPISIL)
US	Steve Knight (NIST) Alain Diebold (Int. SEMATECH)

Metrology Roadmap
2002 Update

US	John Allgair	Motorola
	Alain Diebold	Int. SEMATECH
	Drew Evan	CEA
	David Joy	Univ. of Tenn
	Steve Knight	NIST
	Kevin Monahan	KLA-Tencor
	Noel Poduje	ADE
	Heath Pois	Thermawave
	Bhanwar Singh	AMD
	Andras Vladar	NIST
Speakers		
	Michael Gostein	Philips Analytical
	PY Hung	Int. SEMATECH
	Tom Kelly	Amigo
	Heath Pois	Thermawave
	Benzi Sender	Applied Materials
	Prof. Fred Terry	Univ. of Michigan

AGENDA

- 2002 ITRS Changes
- Lithography Metrology
- FEP Metrology
- Interconnect Metrology
- Materials Characterization
- Key Challenges

2002 ITRS Changes

Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*
MPU / ASIC ½ Pitch (nm)	150	90	65	45	32	22
MPU Printed Gate Length (nm)	90	53	35	25	18	13
MPU Physical Gate Length (nm)	65	37	25	18	13	9
Lithography Metrology						
Printed Gate CD Control (nm) Allowed Litho Variance = 2/3 Total Variance of physical gate length	5.3	3	2	1.5	1.1	0.7
Wafer CD Tool 3σ Precision P/T=0.2 for Printed and Physical Isolated Lines	1.1	0.6	0.4	0.3	0.2	0.1
Line Edge Roughness (nm)	4.5	2.7	1.8	1.3	0.9	0.65
Precision for LER	0.9	0.54	0.36	0.26	0.18	0.13

Orange = production done w/out meeting ITRS precision specification

Interconnect Metrology						
Barrier layer thick (nm) process range (±3σ) Precision 1σ (nm)	13 20% 0.04	10 20% 0.03	7 20% 0.02	5 20% 0.016	4 20% 0.013	
Void Size for 1% Voiding in Cu Lines	87	52	37	26	18	12
Detection of Killer Pores at (nm) size	6.5	4.5	3.25	2.25	1.6	1.1

Metrology Timeline

2003

	2001	2002	2004	2007	2010	2013	2016
Leading Production Technology Node = DRAM ½ Pitch	*130 nm*	*115 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*
MPU / ASIC ½ Pitch (nm)	150	130	90	65	45	32	22
MPU Printed Gate Length (nm)	90	75	53	35	25	18	13
MPU Physical Gate Length (nm)	65	53	37	25	18	13	9

Beta Site
90 nm Node

R&D
65 nm Node

Early R&D
45 nm Node

Leading Edge Tool Specifications set

45 nm Node Metrology R&D Materials available
10 nm structures difficult to obtain

Litho Process part of total CD budget

- Litho Process range - Litho 2/3 Etch 1/3 in 2002
  may change in 2003
- Use Process Range for Physical (Etched) Gate for both Printed and Etched Gate
- Variances add as sum of squares
- Etched Gate
  - 90 nm node Process range for 37 nm physical i.e., etched gate, of 3.7 nm 3σ (i.e. plus or minus 10%)
  - 2/3 of $(3.7\ \text{nm})^2$ = 9.12 nm which gives 3 nm 3σ for Litho Process Range
  - 3σ Precision for P/T of 20% is 0.2 x 3 nm = 0.6 nm
- Make Precision of Printed gate match that of Etched Gate and Result is that Printed Gate now requires better precision

CD Potential Solutions

	2001	2002	2004	2007	2010	2013	2016	
Leading Production Technology Node = DRAM ½ Pitch	*130 nm*	*115 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*	*Driver*
MPU / ASIC ½ Pitch (nm)	**150**	**130**	**90**	**65**	**45**	**32**	**22**	
MPU Printed Gate Length (nm)	**90**	**75**	**53**	**35**	**25**	**18**	**13**	
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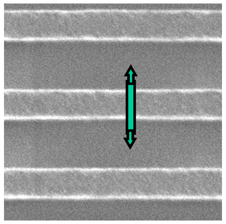
	2001	2002	2004	2007	2010	2013	2016
CD-SEM	🟩	🟧	🟧	🟥	🟥	🟥	🟥
High Voltage CD-SEM				🟥	🟥	🟥	🟥
Scatterometry	🟩	🟧	🟧	🟥	🟥	🟥	🟥
CD-AFM	🟩	🟧	🟧	🟥	🟥	🟥	🟥
Point Projection Microscope e - holography						🟥	🟥

🟥 **R&D Required**

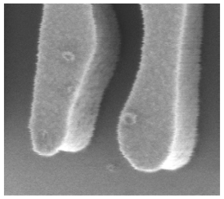
🟧 **Meets ITRS Precision w/o tool matching**

3D CD Metrology SEM – Scatterometry – CD-AFM

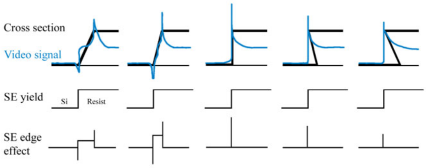
Commercially available

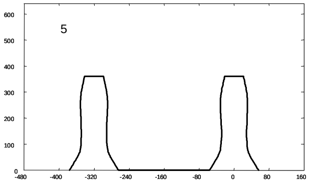


Software comparison of top down line scan of edge to golden image

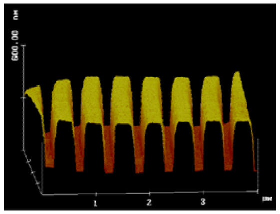


Tilt Beam SEM





Scatterometry



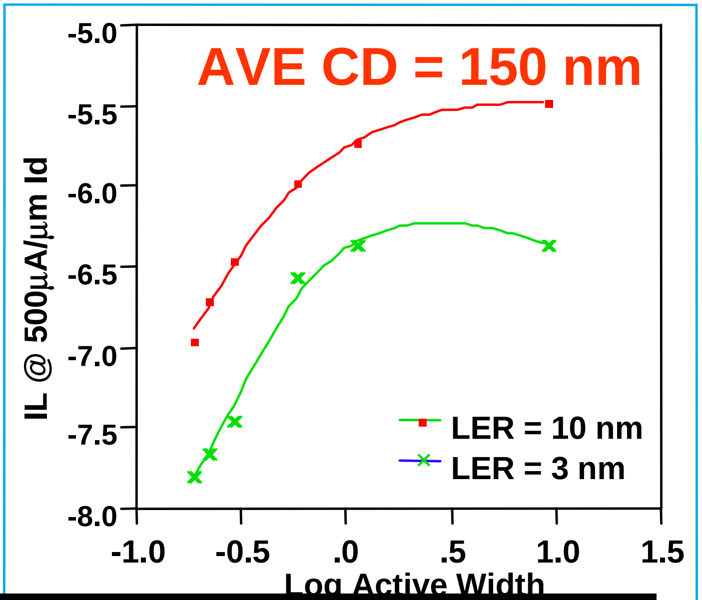
CD-AFM

R&D

Software to convert top down image to 3D image

Line Edge Roughness Requirements

Now: LWR In or Off-line



Line Width Roughness Correlated to Leakage Current Increase

Patterson, et. al., SPIE 2001

Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*
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Thanks to ITRS Litho TWG - Harry Levinson / Mauro Vasconi

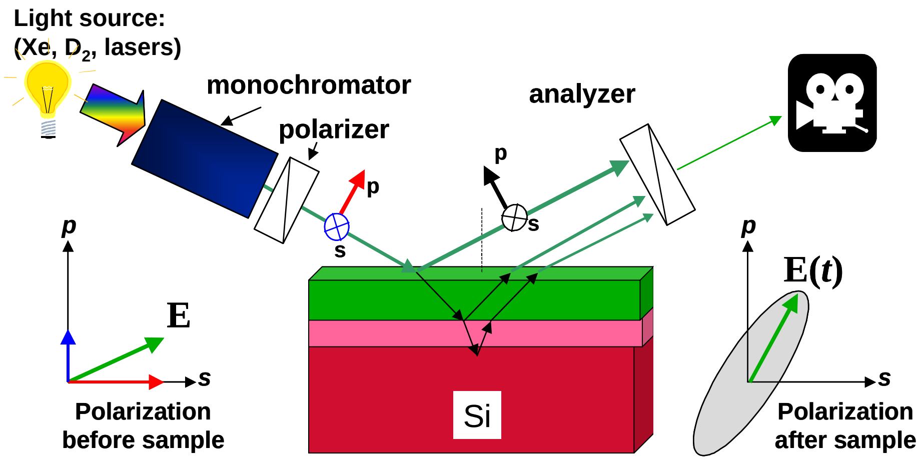
FEP : High κ Metrology

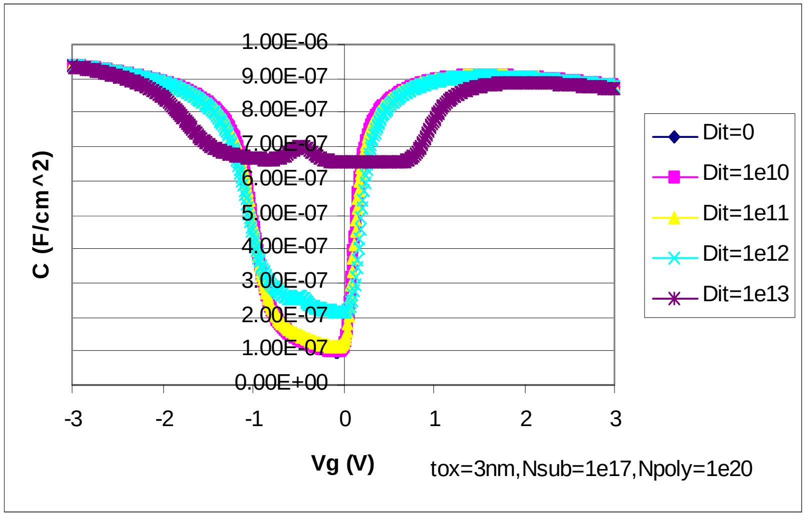
Technology Node	130 nm	90nm	65 nm	45 nm	32 nm	22 nm	Driver
Front End Processes Metrology							
Logic Dielectric Thick Precision 3σ (nm)	0.005	0.004	0.0024	0.0024	0.0016	0.0016	MPU
Metrology for Ultra-Shallow Junctions at Channel Xj (nm)	26	14.8	10	7.2	5.2	3.6	MPU

High κ near UV light absorption
Makes thin interfacial layer difficult to measure

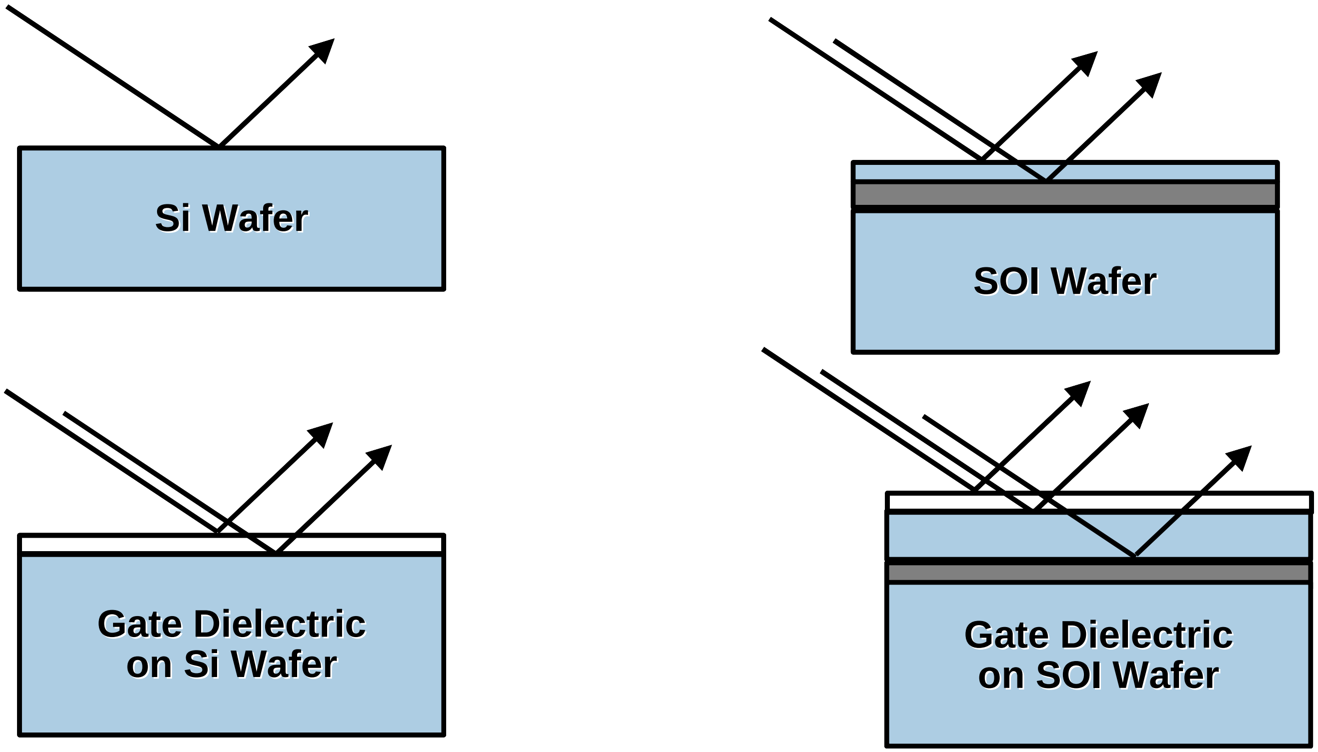
"Out of the Furnace"
High D_{it}

= Error in EOT





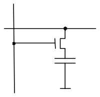
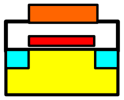
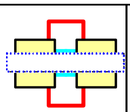
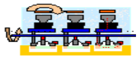
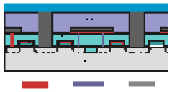
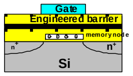
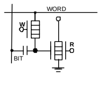
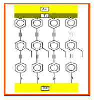
Extra reflection from SOI Wafers Impacts Optical Measurements and Light Scattering



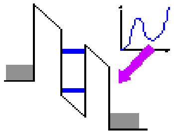
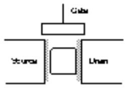
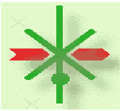
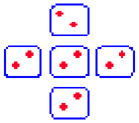
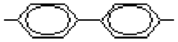
Quantum confinement for sub 20 nm silicon
Need SOI Optical Constants

Metrology & New Structures

Memory

STORAGE MECHANISM	BASELINE 2002 TECHNOLOGIES		MAGNETIC RAM		PHASE CHANGE MEMORY	NANO FLOATING GATE MEMORY	SINGLE/FEW ELECTRON MEMORIES	MOLECULAR MEMORIES
								
DEVICE TYPES	*DRAM*	*NOR FLASH*	*PSEUDO-SPIN-VALVE*	*MAGNETIC TUNNEL JUNCTION*	*OUM*	*-ENGINEERED TUNNEL BARRIER* *-NANOCRYSTAL*	*SET*	*-BISTABLE SWITCH* *-MOLECULAR NEMS* *-SPIN BASED MOLECULAR DEVICES*

Logic

						
Device	Resonant Tunneling Diode – FET	Single Electron Transistor	Rapid Single Quantum Flux Logic	Quantum Cellular Automata	Nanotube Devices	Molecular Devices
Types	**3-terminal**	**3-terminal**	**Josephson Junction +inductance loop**	**-Electronic QCA** **-Magnetic QCA**	**FET**	**2-terminal and 3-terminal**

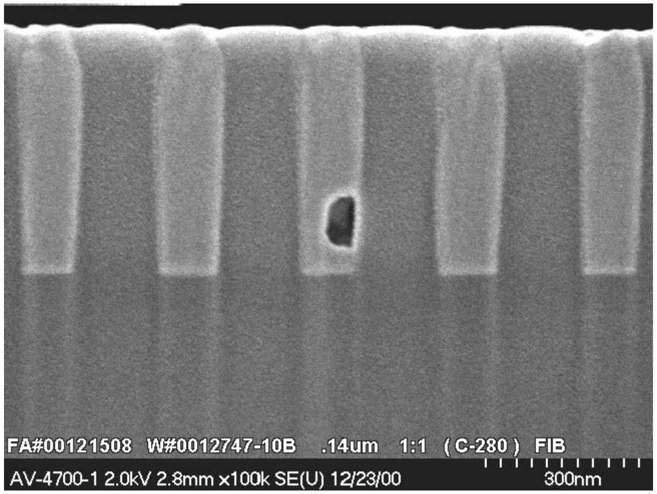
Gaps in Interconnect Metrology

Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*
Interconnect Metrology						
Barrier layer thick (nm) process range (±3σ) Precision 1σ (nm)	**13** **20%** **0.04**	**10** **20%** **0.03**	**7** **20%** **0.02**	**5** **20%** **0.016**	**4** **20%** **0.013**	
Void Size for 1% Voiding in Cu Lines	**87**	**52**	**37**	**26**	**18**	**12**
Detection of Killer Pores at (nm) size	**6.5**	**4.5**	**3.25**	**2.25**	**1.6**	**1.1**

- **VOID Detection in Copper lines**

  now based on ½ via diameter

- **Killer Pore Detection in Low κ**
- **Barrier / Seed Cu on sidewalls**
- **Control of each new Low κ**



High Frequency Measurement of κ

- NIST’s characterization of κ for low κ have shown that κ is stable

- Industry sees less need for high frequency measurement of κ for low κ

Interconnect Clarification for Void Detection in Copper Lines

- Detection of post deposition and anneal process voids at or exceeding listed size (nm) when these voids constitute 1 % or more of total metal level conductor volume of copper line and 5% of vias. [B]

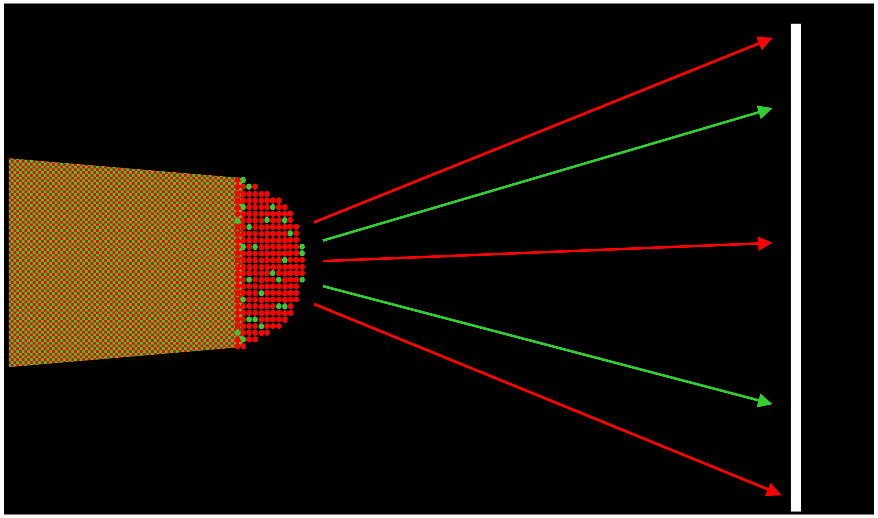
Barrier –Seed Cu Process Tolerance

- Flat – horizontal film measurement used to control sidewall thickness
- Lower limit is thinnest film that acts as barrier
- Upper limit is thickest film allowed for resistivity concerns
- Very thin barriers may be digital
  i.e. there or not

Materials Characterization

Need New Microscopy Methods

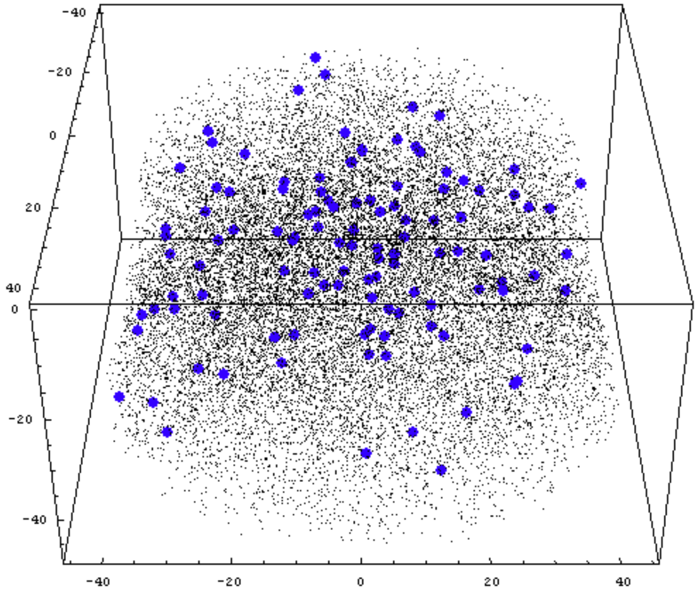
LEAP is one example



LEAP

local electrode atom probe

Atom by atom 3D profile



Key Metrology Challenges

- Breakthrough microscopy for CD measurement
- Measurement capability for control of interface between high κ and substrate & gate electrode
- Low κ killer pore detection and copper void control
- Atom by Atom microscopy for materials characterization

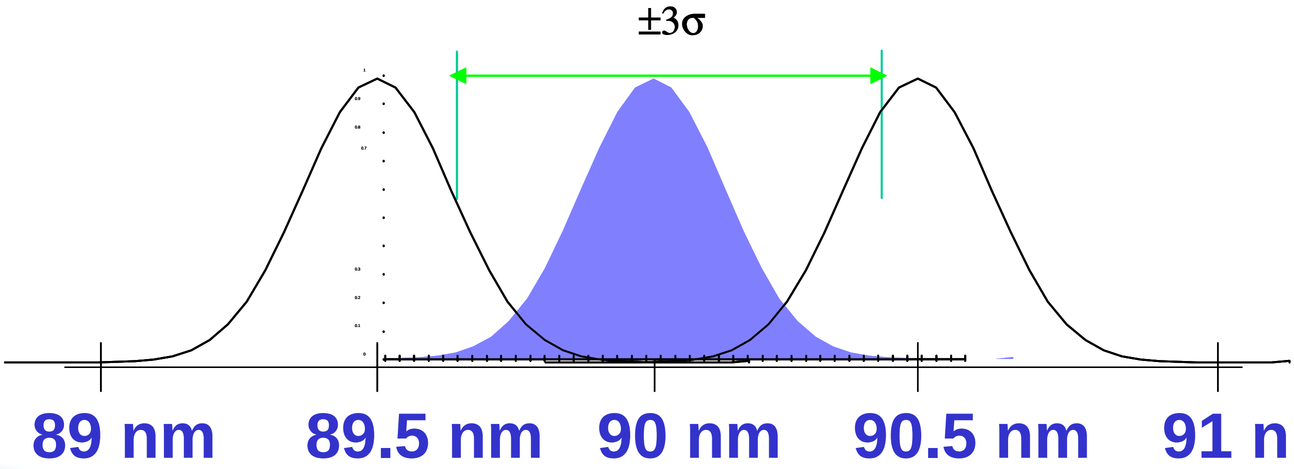
Backup

2001 Metrology Requirements Summary

Technology Node	130 nm	90nm	65 nm	45 nm	32 nm	22 nm	Driver
Lithography Metrology							
Wafer Gate CD nm post-etch contol	6.5	3.7	2.5	1.8	1.3	0.9	MPU
Wafer CD Tool 3s Precision P/T=0.2 Isolated Lines	1.3	0.75	0.5	0.36	0.26	0.18	MPU
Line Edge Roughness (nm)	4.5	2.7	1.8	1.3	0.9	0.65	MPU
Precision for LER	0.9	0.54	0.36	0.26	0.18	0.13	
Overlay Control (nm) (mean +3s)	45	31	26	18	13	9	MPU
Overlay Metrology Precision (nm) P/T=0.1	4.5	3.1	2.6	1.8	1.3	0.9	MPU
Front End Processes Metrology							
Logic Dielectric Thick Precision 3σ (nm)	0.005	0.004	0.0024	0.0024	0.0016	0.0016	MPU
Metrology for Ultra-Shallow Junctions at Channel Xj (nm)	26	14.8	10	7.2	5.2	3.6	MPU
Interconnect Metrology							
Barrier layer thick (nm) process range (±3σ) Precision 1σ (nm)	13 20% 0.04	10 20% 0.03	7 20% 0.02	5 20% 0.016	4 20% 0.013		MPU
Void Size for 1% Voiding in Cu Lines	32.5	22.5	16.25	11.25	8	5.5	MPU
Detection of Killer Pores at (nm) size	6.5	4.5	3.25	2.25	1.6	1.1	MPU

New Metrology Need: Standardized Statistics for Discretized Data

- Some new methods fit measurement to a discrete set of possible results
- This could result in artificially good precision values that do not really evaluate process control capability



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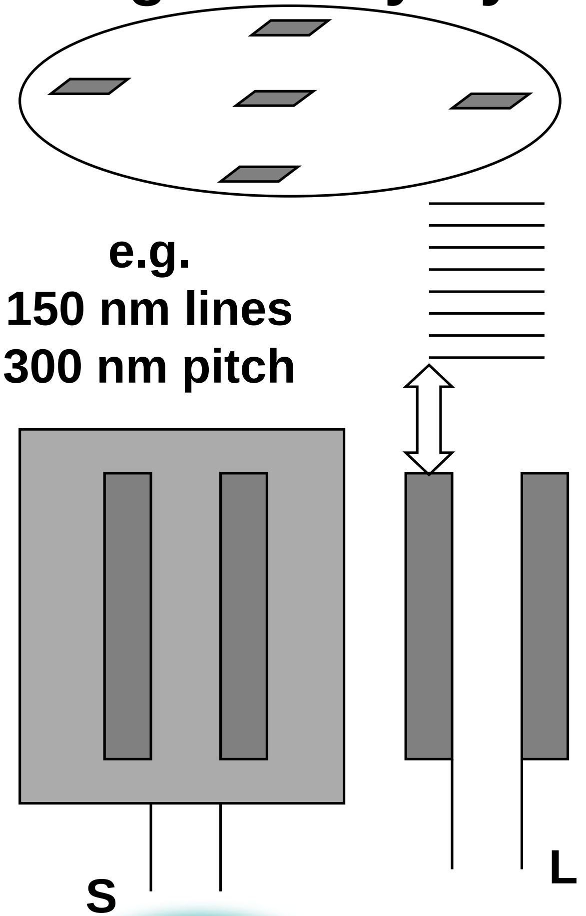
Capacitor Thickness Precision 3σ (nm)	0.05	0.05	0.11	0.11	0.09	0.07	DRAM
Metrology for Ultra-Shallow Junctions at Channel Xj (nm)	26	14.8	10	7.2	5.2	3.6	MPU
Interconnect Metrology							
Barrier layer thick (nm) process range (±3σ) Precision 1σ (nm)	18 20% 0.06	11 20% 0.036	8 20% 0.027	7 20% 0.023	5 20% 0.017	4 20% 0.01	MPU
Void size for 1 % Voiding in Copper Lines	32.5	22.5	16.25	11.25	8	5.5	MPU
Detection of Killer Pore at (nm) Size	6.5	4.5	3.25	2.25	1.6	1.1	MPU

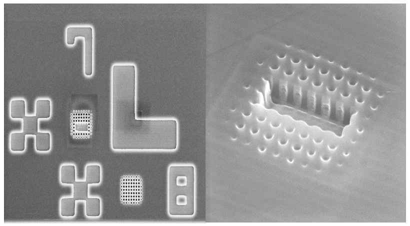
Novel Methods for FEM control

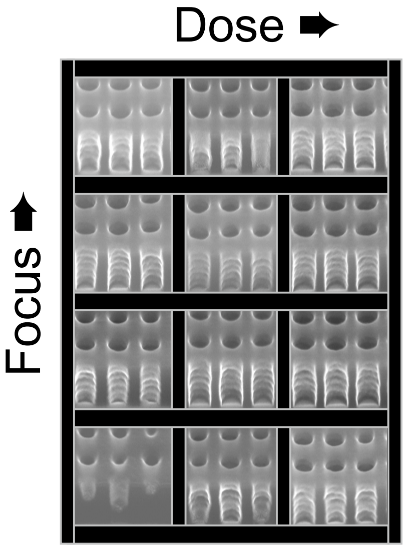
Optical CD
using Overlay System



e.g.
150 nm lines
300 nm pitch

Dualbeam FIB
FEI



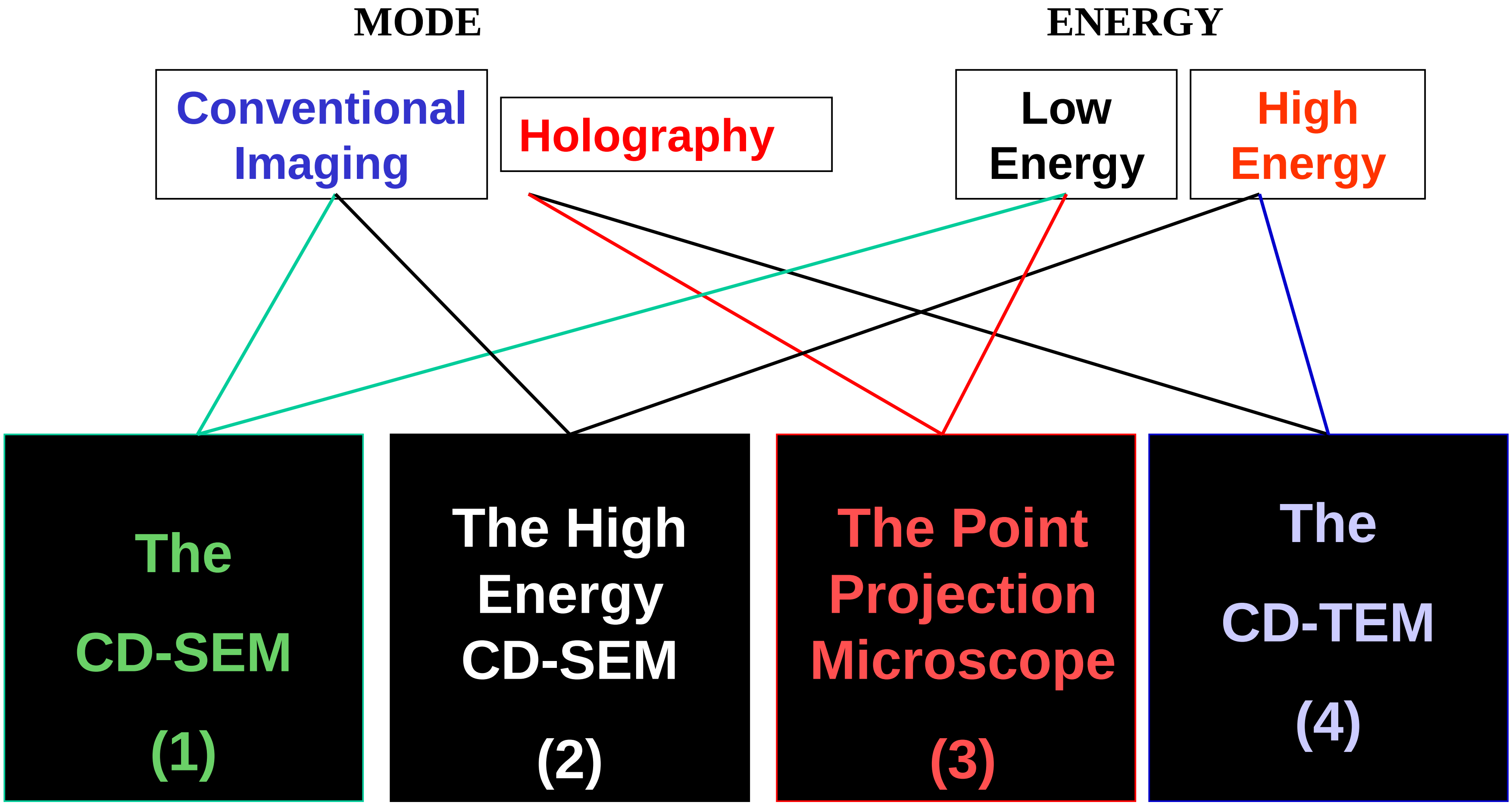


Automatic cross-sectioning, imaging and metrology from all sites of the FEM

Status of Potential Solutions for CD

- Single tool remove matching precision loss
- CD-SEM supplier community expresses confidence enhancements can extend traditional approach
- Real Time Scatterometry replaces library approach
- Scatterometry may require VUV
- CD-AFM tip technology limits dense line and contact measurement

CD-SEM Possibilities



MODE

ENERGY

Conventional Imaging

Holography

Low Energy

High Energy

The CD-SEM (1)

The High Energy CD-SEM (2)

The Point Projection Microscope (3)

The CD-TEM (4)

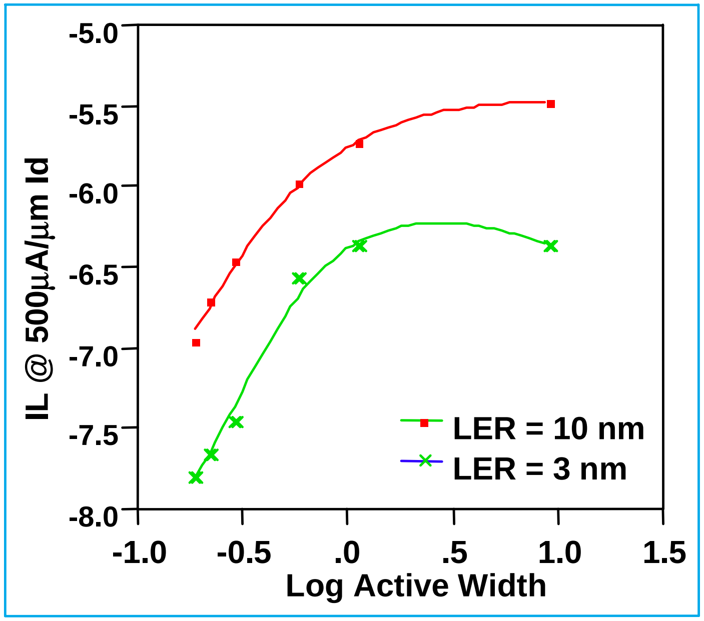
Leakage Current correlated to Line Edge Roughness

Center of data at 150 nm channel length with drive current of 500 µA/µm

Leakage plotted versus active width of transistor

The two lines show the dependence for the case of low and high line edge roughness.

Units for leakage current are A/µm, plotted on a logrithimic scale



Patterson, et. al., SPIE 2001

Thanks to ITRS Litho TWG - Harry Levinson / Mauro Vasconi

CD-SEM a Potential Solution for Wafer and Mask / R&D + Production

Barriers and Solutions

193 & 157 nm Resist Damage

» lower dose images

Lineshape

» tilt beam SEM vs software

Precision Improvements

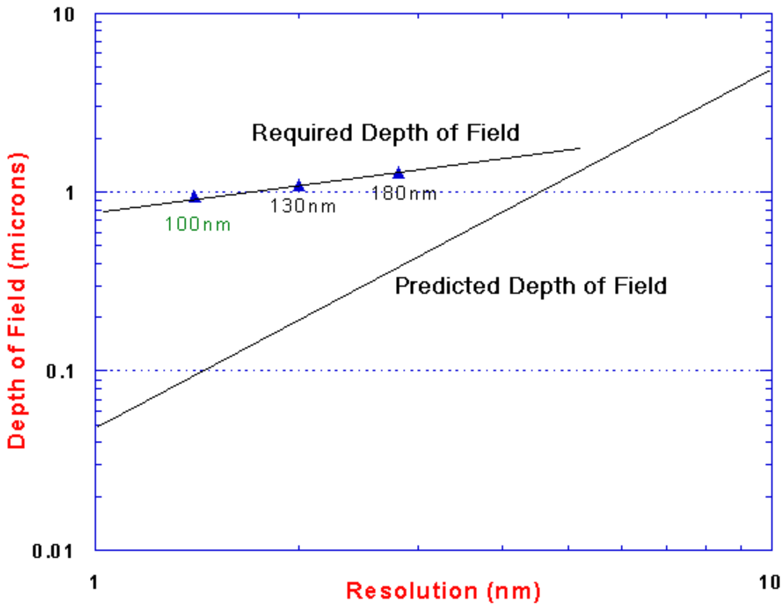
» new nano-tip source

Depth of Focus

» new SEM concept needed

Ultimate Limit of CD-SEM

» ~ 5 nm for etched poly Si Gate



Sato and Mizuno, EIPBN 2000, Palm Springs, CA

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- **Physical Metrology for high k gate stack**
  - **Optical Models for next High k (beyond HfO2)**
  - **Interfacial control for interface between high k and silicon**
- **Electrical Metrology for high k gate stack**
  - **Application of Non-contact C-V to next High k (beyond HfO2)**
  - **Comparison of non-contact electrical to C-V**

FEP Metrology

- Optical and Electrical measurement of High κ can be done for development but needs to be robust for manufacturing

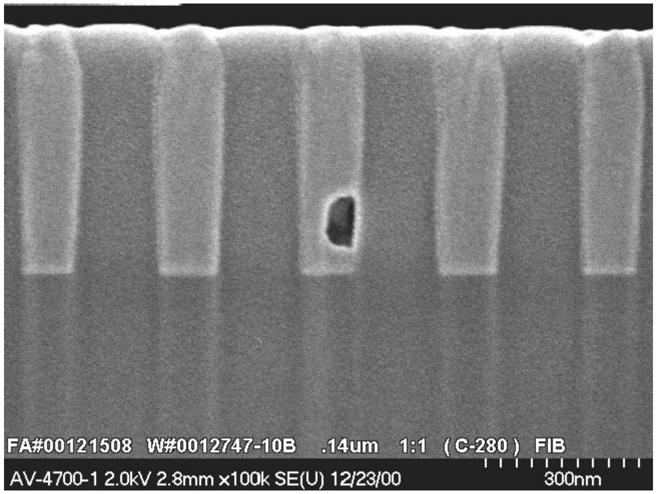
- Metrology for interface below High κ needs R&D

- USJ Metrology needs development for < 65 nm

- FERAM needs fatigue testing for 10^{16} read/write cycles

Voids in Copper
Pore Size/Killer Pores in Low k

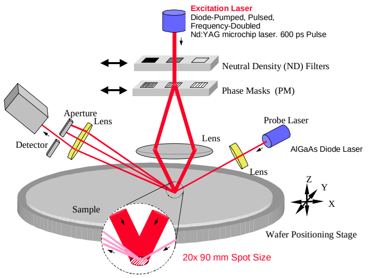
- Random isolated void detection in copper lines may be used in development at levels above the < 1% metric



- <1% may not be measurable

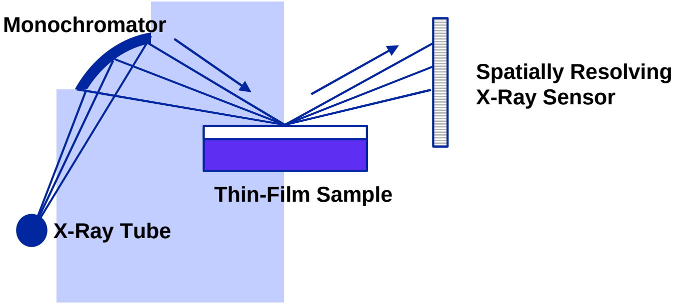
Interconnect Metrology Solutions

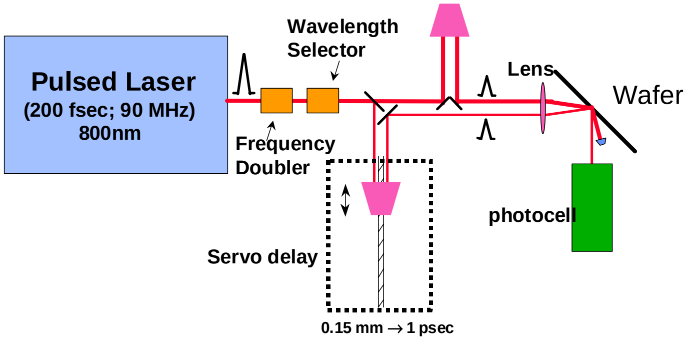
Barrier/Seed Cu Films

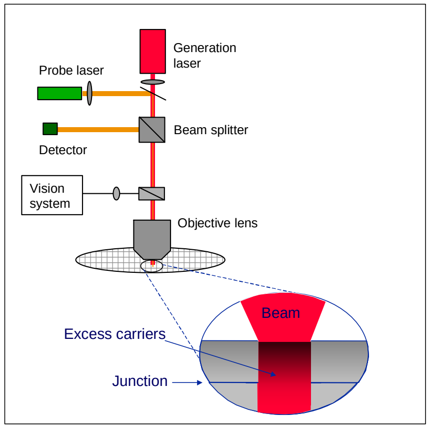


~1-2 seconds/point (measurement + data analysis + stage motion)

Acoustic ISTS
Picosecond acoustics
X-ray reflectivity
X-ray fluorescence
Non-contact resistivity







5 Potential Solutions
all expected to meet precision requirements
some are extendable to patterned wafers

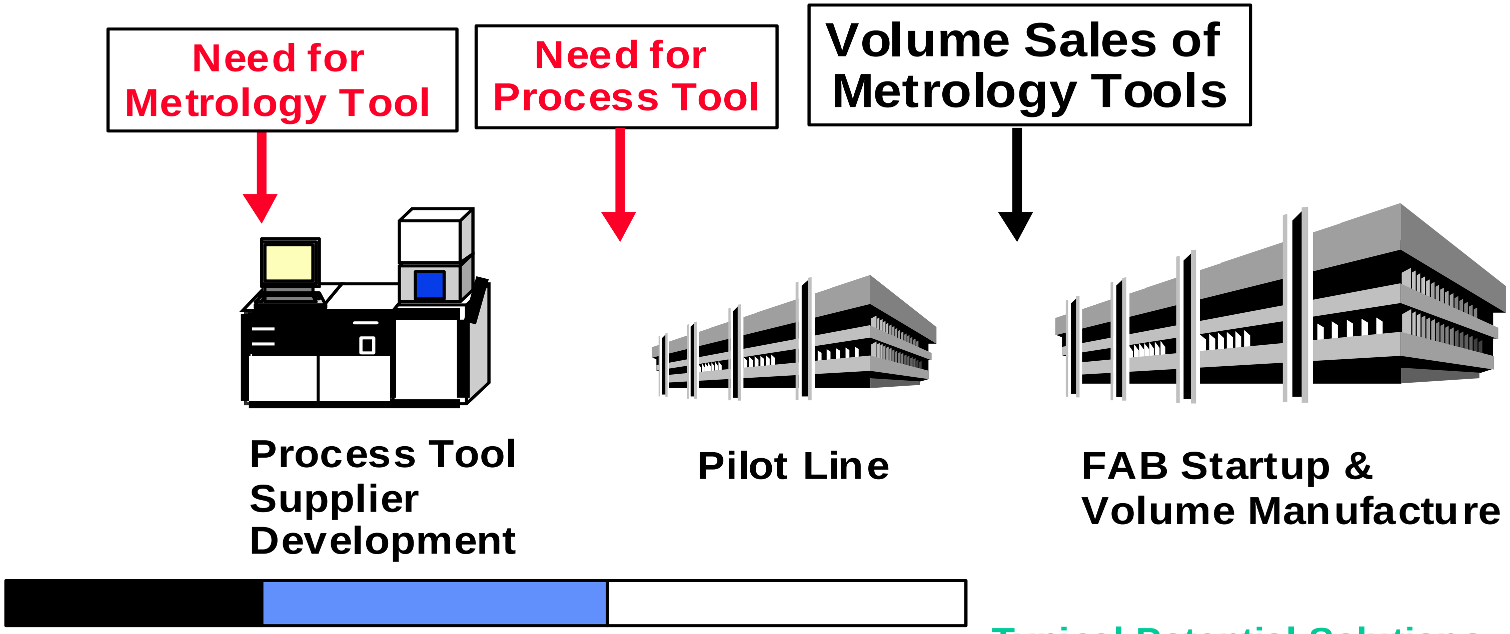
2001 Grand Challenges

- Development of Metrology tools in time.
- Rapid non-destructive metrology for CD, overlay, defect detection and line edge roughness that meets ITRS timing and technology requirements.

Will Market Risks allow for innovation?

Metrology Timing vs Infrastructure Capabilities

Gap in long term R&D Spending + Development Funding Model



Need for Metrology Tool

Need for Process Tool

Volume Sales of Metrology Tools

Process Tool Supplier Development

Pilot Line

FAB Startup & Volume Manufacture

Research Required

Development Underway

Qualification/ Preproduction

Typical Potential Solutions Time Line for Process Tool