

# Interconnect Working Group

**ITRS 2002**



**4 December 2002**  
**Tokyo**



**International Technology Roadmap for Semiconductors**

*4 December 2002, ITRS 2002 Update Conference*

# ITWG Regional Chairs

## Japan

Shinichi Ogawa

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## Taiwan

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## Korea

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## US

Robert Geffken

Christopher Case

## Europe

Hans Joachim-Barth

Joachim Torres

December 03, 2002 Meeting

Akihiko Ohsaki

Shinichi Ogawa

Tomoji Nakamura

Kazuyoshi Ueno

Hideki Shibata

Chris Case



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# Agenda

- Interconnect scope
- Highlight of changes
- Difficult challenges
  - Review of key issues on materials
- Reliability
- Technology requirements issues
  - Table updates
- 2003 section preview
- Last words

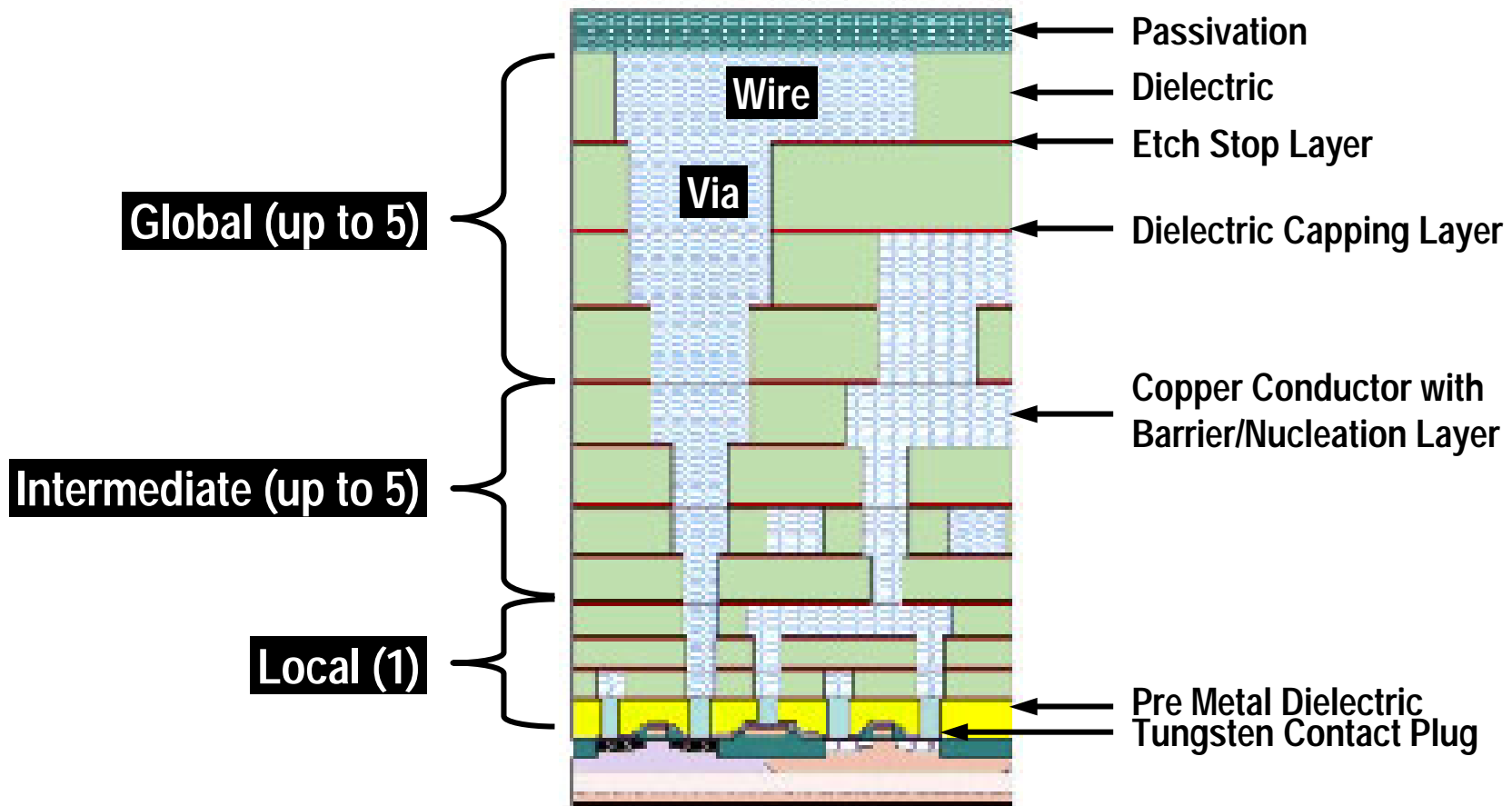


# Interconnect scope

- Conductors and dielectrics
  - local through global levels
  - Starts at PMD
- Associated planarization
- Necessary etch, strip and clean
- Embedded passives
- Reliability and system and performance issues
- Ends at the top wiring bond pads
- Predominantly “needs” based



# Typical chip cross-section illustrating hierarchical scaling methodology



# 2002 highlights

- No significant changes
  - No changes to timing
  - No changes to number of metal levels
  - No changes to low k dielectric roadmap
- New wiring performance metrics
- Updated  $J_{max}/I_{max}$
- Clarification of global wiring pitch
- Increased emphasis on reliability issues associated with Cu/low k integration



# Difficult Challenges

>65 nm

- **Introduction of new materials\***
- **Integration of new processes and structures\***
- Achieving necessary reliability
- Attaining dimensional control
- Manufacturability and defect management that meet overall cost/performance requirements

<65 nm

- Dimensional control and metrology
- Patterning, cleaning and filling high aspect ratios features
- Integration of new processes and structures
- Continued introductions of new materials and size effects
- **Identify solutions which address global wiring scaling issues\***



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# Introduction of new materials

Near term

“Barrier Engineering”

new barriers and nucleation layers

*in situ* formed dielectric and metal

ALD potential solutions

porous dielectrics

Combination of materials and technologies

Lack of interconnect/packaging architecture design

optimization tool



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# Materials Challenges

Long term

Continued introduction of materials

barriers/nucleation layers for alternate conductors -  
optical, low temp, RF, air gap

alternate conductors, cooled conductors

More reliability challenges

Microstructural and atom scale effects



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# Reliability Challenges

## Short term

Electrical, thermal and mechanical exposure

New failure mechanisms with Cu/low k present significant challenges before volume production

- interface diffusion

- interface delamination

Higher intrinsic and interface leakage in low k

Need for new failure detection methodology to establish predictive models



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# Dimensional Control

3D CD of features

performance and reliability implications

Void detection in Cu wires

Multiple levels

reduced feature size, new materials and pattern dependent processes

process interactions

CMP and deposition - dishing/erosion - thinning

Deposition and etch - to pattern multi-layer dielectrics

Aspect ratios for etch and fill

particularly DRAM contacts and dual damascene



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# Process Integration

Combinations and interactions of new materials and technologies  
interfaces, contamination, adhesion, diffusion, leakage concerns,  
thermal budget, ESH, CoO

Structural complexity

levels - interconnect, ground planes, decoupling caps

passive elements

mechanical integrity

other SOC interconnect design needs (RF)

cycle time



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# Technology Requirements

- Wiring levels including “optional levels”
- Reliability metrics
- Wiring/via pitches by level
- Performance metric
- Planarization requirements
- Conductor resistivity
- Barrier thickness
- Dielectric metrics including effective  $\kappa$



# MPU HP Near Term Years

YEAR TECHNOLOGY NODE	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm) (Sc. 2.0)	130	115	100	90	80	70	65
MPU/ASIC ½ PITCH (nm) (Sc. 3.7)	150	130	107	90	80	70	65
Local wiring pitch (nm)	350	295	245	210	185	170	150
<b>*Interconnect RC delay 1 mm line (ps) [3]</b>	<b>86</b>	<b>121</b>	<b>176</b>	<b>198</b>	<b>256</b>	<b>303</b>	<b>342</b>
<b>*Line length where <math>\tau = RC</math> delay (<math>\mu m</math>)</b>	<b>137</b>	<b>106</b>	<b>80</b>	<b>70</b>	<b>57</b>	<b>50</b>	<b>44</b>
Minimum global wiring pitch (nm)	670	565	475	460	360	320	290
Ratio (global wiring pitch/intermediate wiring pitch)	1.5 - 5.0	1.5 - 5.0	1.5 - 5.0	1.5- 6.7	1.5 - 6.7	1.5 - 6.7	1.5 - 8.0

New RC delay metric for a 1 mm line (level dependent)

Ratio of global wiring pitch to semi-global wiring pitch



# MPU HP Near Term Years

YEAR TECHNOLOGY NODE	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm) (SC. 2.0)	130	115	100	90	80	70	65
MPU/ASIC ½ PITCH (nm) (SC. 3.7)	150	130	107	90	80	70	65
MPU PRINTED GATE LENGTH (nm) (SC. 3.7)	90	75	65	53	45	40	35
MPU PHYSICAL GATE LENGTH (nm) (SC. 3.7)	65	53	45	37	32	28	25
Conductor effective resistivity ( $\mu\Omega$ -cm) Cu intermediate wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (for Cu intermediate wiring) (nm)	16	14	12	10	9	8	7
Interlevel metal insulator —effective dielectric constant ( $\kappa$ )	3.0-3.6	3.0-3.6	3.0-3.6	2.6-3.1	2.6-3.1	2.6-3.1	2.3-2.7
Interlevel metal insulator (minimum expected) —bulk dielectric constant ( $\kappa$ )	<2.7	<2.7	<2.7	<2.4	<2.4	<2.4	<2.1

Bulk and effective dielectric constants described

Unchanged from 2001 – differing views

Cu at all nodes - conformal barriers



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# MPU HP Long Term Years

Conductor effective resistivity (red) because of scattering effects - research required

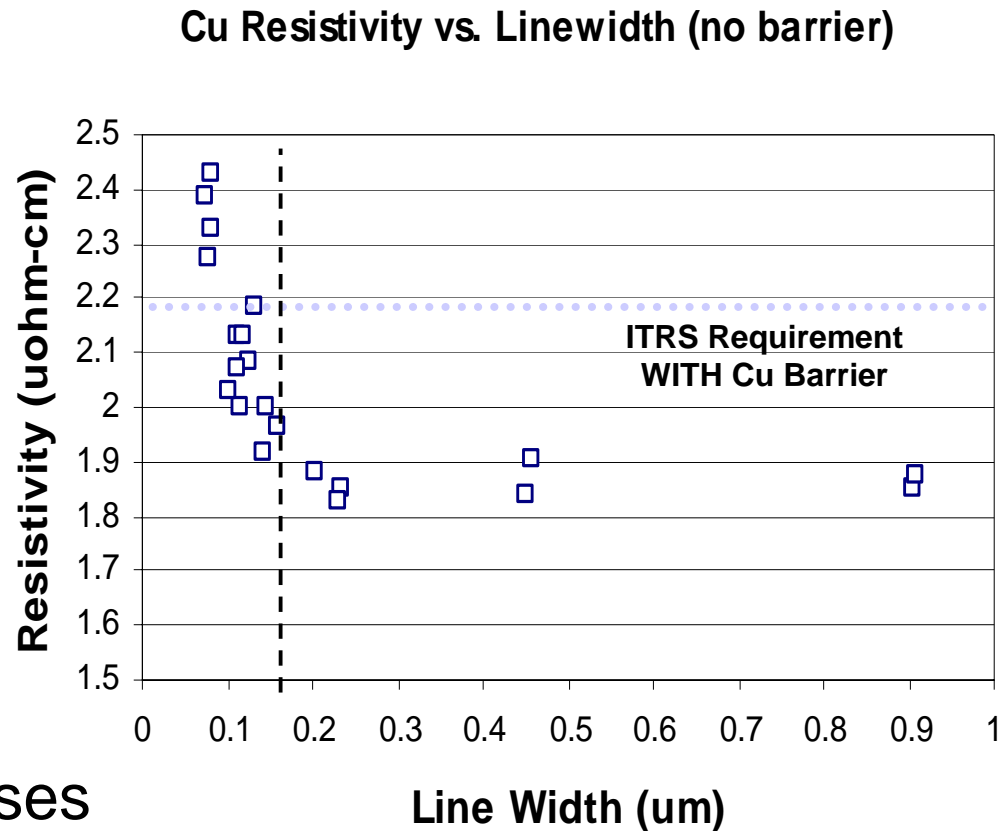
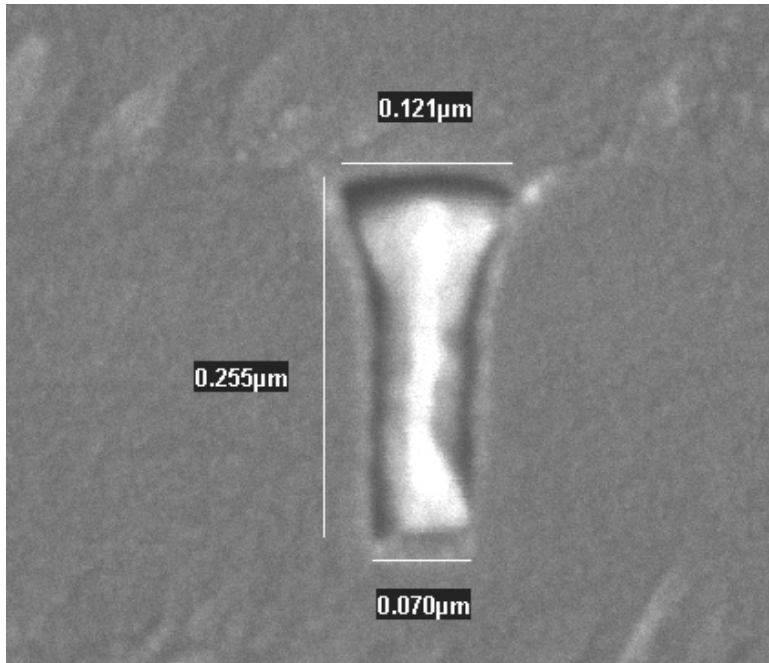
Zero thickness barrier desirable but not required

Seeking new metric for barrier

YEAR TECHNOLOGY NODE	2010	2013	2016
DRAM 1/2 PITCH (nm) (Sc. 2.0)	45	32	22
MPU/ASIC 1/2 PITCH (nm) (Sc. 3.7)	45	32	22
MPU PRINTED GATE LENGTH (nm) (Sc. 3.7)	25	18	13
MPU PHYSICAL GATE LENGTH (nm) (Sc. 3.7)	18	13	9.0
Number of metal levels	10	11	11
Total interconnect length (m/cm <sup>2</sup> ) – active wiring only, excluding global levels (footnote for calculation)	16063	22695	33508
Local wiring pitch (nm)	105	75	50
Local A/R (for Cu)	1.8	1.9	2.0
Intermediate wiring pitch (nm)	135	95	65
Intermediate wiring dual damascene A/R (Cu wire/via)	1.8/1.6	1.9/1.7	2.0/1.8
Minimum global wiring pitch (nm)	205	140	100
Global wiring dual damascene A/R (Cu wire/via)	2.3/2.1	2.4/2.2	2.5/2.3
Cu thinning global wiring due to dishing (nm), 100 micron wide feature	14	10	8
Conductor effective resistivity (μΩ-cm) Cu intermediate wiring*	2.2	2.2	2.2
Barrier/cladding thickness (for Cu intermediate wiring) (nm)***	5	3.5	2.5
Interlevel metal insulator—effective dielectric constant (κ)	2.1	1.9	1.8
Interlevel metal insulator (minimum expected)—bulk dielectric constant (κ)	<1.9	<1.7	<1.6



# Effect Of Line Width On Cu Resistivity



Conductor resistivity increases  
expected to appear around 100 nm linewidth -  
will impact intermediate wiring first - ~ 2006

Courtesy of SEMATECH



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# DRAM Near Term Years

YEAR TECHNOLOGY NODE	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm) (Sc. 2.0)	130	115	100	90	80	70	65
MPU/ASIC ½ PITCH (nm) (Sc. 3.7)	150	130	107	90	80	70	65
Number of metal levels	3	3-4	4	4	4	4	4
Contact A/R—stacked capacitor	11	12	13	15	15	16	16
Local wiring pitch (nm) noncontacted	260	230	200	180	160	150	130
Specific contact resistance ( $\Omega\text{-cm}^2$ )	1.7E-07	1.4E-07	1.0E-07	8.5E-08	7.0E-08	5.0E-08	4.0E-08
Specific via resistance ( $\Omega\text{-cm}^2$ )	2.0E-09	1.5E-09	1.1E-09	9.0E-10	7.5E-10	5.8E-10	5.0E-10
Conductor effective resistivity ( $\mu\Omega\text{-cm}$ )*	3.3	3.3	3.3	2.2	2.2	2.2	2.2
Interlevel metal insulator— effective dielectric constant ( $\kappa$ )	4.1	3.0–4.1	3.0–4.1	3.0–4.1	3.0–4.1	2.6–3.1	2.6–3.1

Small changes in A/R, specific via and contact resistance

Contact A/R rises to >20 in 2016 - a red challenge - associated with 44 nm non-contacted local wiring pitch

Low k usage precedes Cu by two years



# Preview 2003

- Barriers/Nucleation Layers
- Conductors
- Etch, Strip and Cleans



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# Barriers/Nucleation Solutions

- Barrier engineering approaches
  - for porous low k
  - For Cu resistivity control
    - Potential solutions address thin conformal layer
      - atomic layer deposition – ALD
      - Feature smoothing
- ECD and Electroless
  - ALD or CuCVD nucleation layers
  - Seed repair
  - Direct ECD on barriers
  - electrolyte management
  - electroless capping layers (barrier) post damascene polish
- New cleans



# Conductor Potential Solutions

Conductor Potential Solutions											
First Year of IC Production	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011
<b>Local Wiring</b>											
Seamless fill W conductor	█										
High A/R CVD W contact fill for DRAM	█	█	█	█	█	█	█				
Enhanced PVD/CVD Al fill											
<b>Intermediate Wiring</b>											
ECD Cu	█	█	█	█	█	█	█				
ECD Cu enhancements (combinations w/with CMP and CEP)	█	█	█	█	█	█	█				
CVD Cu							█				
CVD/PVD Cu variants											
Low resistivity Cu process*	█	█	█	█	█	█	█	█	█		
<b>Global Wiring</b>											
Cooled conductors	█	█	█	█	█	█	█				
Superconductors								█	█		
RF											
Optical											
<b>Passives</b>											
Electrode materials for metal-insulator-metal capacitors	█	█									
Magnetic materials for inductors	█	█	█								
*Cu process with optimized interfaces, microstructure and impurities to alleviate resistivity rise at small critical dimensions											

## Challenges and changes

Seamless fill W conductor  
 -ALD W nucleation for W  
 -ALD TiN for contact fill

Low resistivity Cu process needed to address resistivity increases - address the interface issues  
 Doped Cu

Cu ECD/CEP combinations

Conductors, etch, dielectrics and planarization should address novel cleans



# Etch/Strip/Cleans Potential Solutions

First Year of IC Production	2001	2003	2005	20
<b>ETCH</b>				
<b>Metal Etch</b>				
New electrode material for high k				
Other				
<b>DIELECTRIC ETCH OF CONTACT / VIA / TRENCH</b>				
High k materials				
Moderate k materials				
Standard k (SiO <sub>2</sub> , Si <sub>3</sub> N <sub>4</sub> )				
Standard k (SiC)				
Low k materials				
Ultra Low k materials				
Extreme Low k materials				
<b>Ferroelectrics</b>				
PZT, SBT				
<b>STRIP AND RESIDUE REMOVAL</b>				
<b>CLEANS</b>				
Post metal etch cleans				
Integrated wet and dry solutions				
SCCO <sub>2</sub> with copolymer				
Ozone combined gas/liquid approaches				
	<span style="display: inline-block; width: 15px; height: 10px; background-color: black; margin-right: 5px;"></span> Research Required <span style="display: inline-block; width: 15px; height: 10px; background-color: blue; margin-left: 20px; margin-right: 5px;"></span> Development Underway			

## Challenges and changes

- Etch is now driven by new materials and integration schemes
  - Alternative etch gases
    - Distinguished by level and function
    - MRAM, FERAM, passives
- Many new low and high k materials - may require new chemistries - supercritical CO<sub>2</sub>/solvents, ozone gas/liquid approaches
- Dimensional control with small features and high A/R
- Selectivity to etch stops and hard masks
- Chamber cleans



# Solutions beyond Cu and low $\kappa$

Material innovation combined with traditional scaling will no longer satisfy performance requirements

Design, packaging and interconnect innovation needed

Alternate signal transmission media

optical, RF

Emerging devices (3D or multi-level) in the interconnect



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# Last words

Continued rapid changes in materials

Develop solutions for emerging devices

Must manage 3D CD

System level solutions must be accelerated to address the global wiring grand challenge

Cu resistivity increase impact appears ~2006

materials solutions alone cannot deliver performance - end of traditional scaling

integrated approach with design and packaging



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