ITRS 2002 Update Conference

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Tokyo, JAPAN

Front End Processes

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FEP Technology Working Groups

- **Starting Materials**
- **Surface Preparation**
- **Thermal Films**
- **Doping**
- **Critical Dimension Etch**
- **Memory**
  - **DRAM Stack Capacitor**
  - **DRAM Trench Capacitor**
  - **Flash Memory**
  - **FeRAM**

Starting Materials

2002 Updates

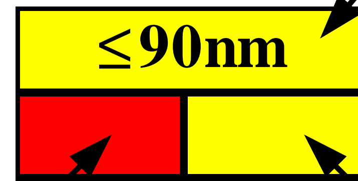
–Minor text corrections

–Update Cell Keys for supplier capability and metrology readiness

Cell Key Example:Site Flatness (2004, 90nm node)

Technology **requirements value** & supplier **manufacturing capability**

White: Solutions Exist
Yellow: Solutions are known
Red: Solutions are NOT known



Criticality of requirement to IC wafer user

White: Maintenance
Yellow: Improvement necessary
Red: "Showstopper"

Metrology readiness capability

White: Metrology Exist
Yellow: Improvement necessary
Red: "Showstopper"

Starting Materials Proposed 2003 Projects

- **Next Generation Starting Materials beyond 300mm**
  - **450mm wafer size?**
  - **Cost-effective wafer manufacturing**
  - **Alternate *Si on X* substrate materials?**
- **Update SOI requirements**
- **Update Starting Substrate Defect Densities**

  to reflect updated DRAM and MPU active areas.
- **Sub TWG(new) will address strained-Si:Ge**
  - **SOI-like structures appear to be preferred for enhanced device performance.**

Surface Preparation

2002 Updates

1 Particles → Minor corrections due to calculation errors

Was	Particles (#/wafer)	63	94	60	83	48	66	39	D ½
Is	Particles (#/wafer)	62	92	59	83	48	66	39	D ½

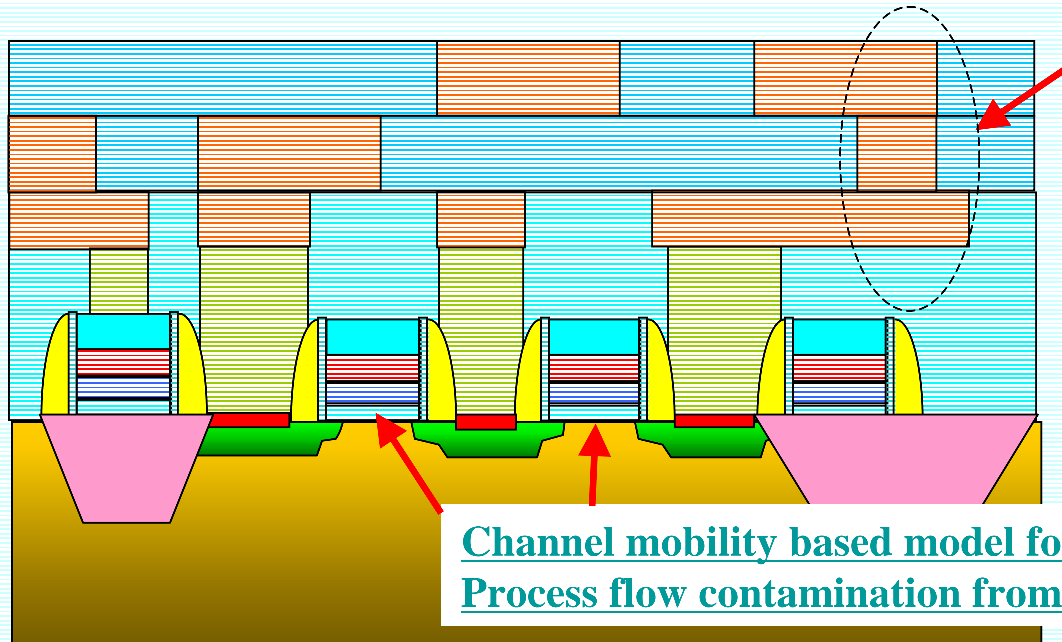
2 Residual interfacial Oxygen → Partially oxidized surfaces should be avoided

Was	Residual interfacial oxygen (O at/cm2)	<1E14	<1E14	<1E14	<1E14	<1E14	<1E14	<1E14	D ½, M
Is	Residual interfacial oxygen (O at/cm2)	<1E14	<1E13	<1E13	<1E13	<1E13	<1E13	<1E13	D ½, M

Surface Preparation

2003 Projects

Review drivers for critical metals



BEOL surface preparation models and requirements:

1 Low-k damage
2 CD and profile shifts
3 Copper contamination
4 Copper removal from via bottom

Channel mobility based model for surface roughness
Process flow contamination from high-k materials

Backside particle model and requirements

Thin Film Technology Requirements

Lg is slowed by one year for LSTP !

		01	02	03	04	05	06	07	10	13	16
MPU/ ASIC	Lg	65	53	45	37	32	28	25	18	13	9
	EOT	1.3-1.6	1.2-1.5	1.1-1.4	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
	Ig (nA/um)	10	30	70	100	300	700	1000	3000	7000	10000
LOP	Lg	90	75	65	53	45	37	32	22	16	11
	EOT	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4	0.8-1.2	0.7-1.1	0.6-1.0
	Ig (nA/um)	0.1	0.1	0.1	0.3	0.3	0.3	0.7	1	3	10
LSTP	Lg	100	90	75	65	53	45	37	28	20	16
	EOT	2.4-2.8	2.2-2.6	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	0.9-1.3	0.8-1.2	0.7-1.1
	Ig (pA/um)	1	1	1	1	1	1	1	3	7	10

Drastic Reduction of gate dielectric EOT

EOT (nm)

3.0
2.0
1.0
0.0

LSTP

Gate leakage!

Gate leakage!

Drive high-k

HP

LOP

Process controllability & Reliability!

2000
2005
2010
2015
2020

Year

2003 Thermal Films Projects

- **Update gate leakage models and requirements forecasts together with PIDS TWG**

- **Update gate dielectric potential solutions to reflect current understanding**

Doping - 2002 Updates

- Correction of out-year polysilicon doping errors

	Table 51b Thermal & Thin Film, Doping and Etching Technology Requirements—Long-term				
	Year of Production	2010	2013	2016	Driver
Was	Active poly doping for 25% depletion allowance (cm^{-3}) [S]	1.80E+20	2.50E+20	2.99E+20	MPU/ASIC
Is	Active poly doping for 25% depletion allowance (cm^{-3}) [S]	2.50E+20	2.99E+20	3.74E+20	MPU/ASIC

- Add- Drain extension sheet resistance requirements for N-channel MOSFET (only p-MOSFET was shown in 2001)

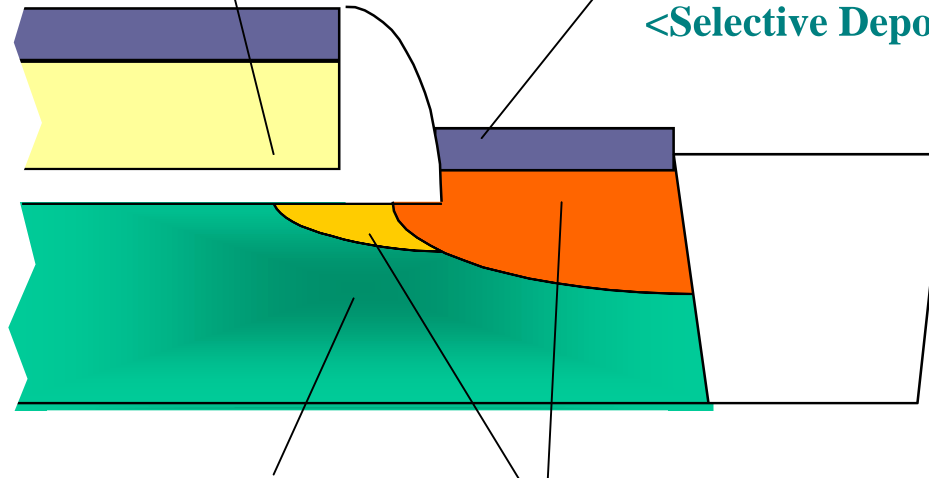
	Year of Production	2001	2002	2003	2004	2005	2006	2007	Driver
Add	Maximum drain extension sheet resistance (NMOS) (Ω/sq) [H]	190	220	260	310	360	390	360	MPU/ASIC

	Year of Production	2010	2013	2016	Driver
Add	Maximum drain extension sheet resistance (NMOS) (Ω/sq) [H]	390	440	570	MPU/ASIC

2003 Doping Technology Requirements and Potential Solutions

Active Poly Doping
<Poly-SiGe/ Dual Metal>

Contact on Ultrashallow Junction
Minimizing Silicon Consumption
<Selective Deposited Silicide/ Metal>



Red:
Update Modeling

Vertical and Lateral Channel Engineering
<Abruptly Doped Epi Channels>

High Activation of Dopant
Shallow / Low Resistance Drain Extension
Lateral and Vertical Abruptness
<Spike/ Impulse Anneal
Undoped or Doped Epi/Poly,
Solid/Gas Phase Doping>

Critical Dimension Etch

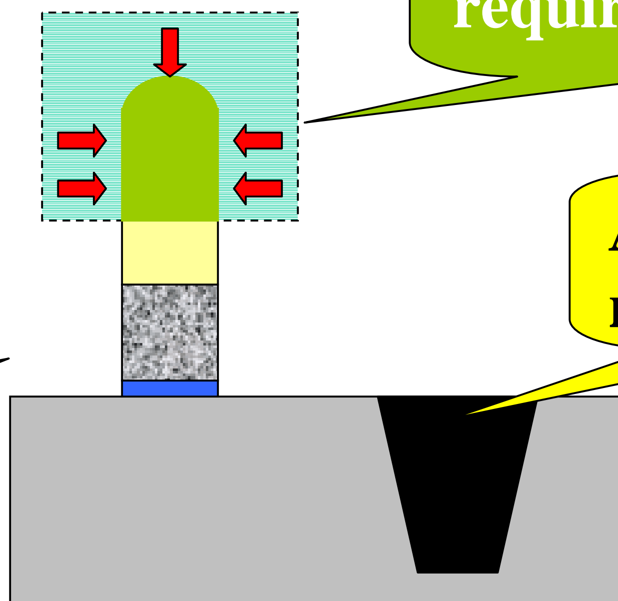
No year 2002 updates

2003 Projects

Upgrade resist trim and etch CD requirements

$$\frac{(\sigma_{trim\&etch})^2}{(\sigma_{total})^2} = \frac{1}{3} \rightarrow \frac{1}{5}$$

Guidance on etcher repeatability



Update Resist Trim requirements

Add STI Etch requirements

DRAM Stacked Capacitor

No year 2002 updates

2003 Projects

Potential delay in cell “a” factor reduction from eight to six

→ Re-examine storage Capacitor parameters and other storage node parameters

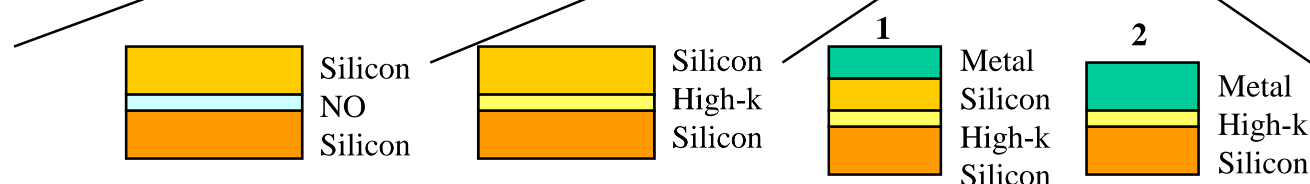
DRAM Trench Capacitor

2002 updates

Updated because of need to achieve higher storage capacitance and lower sheet resistance

Table 53a DRAM Trench Capacitor Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Was	*Upper electrode*	**Poly-Silicon**	**Poly-Silicon**	**Poly-Silicon**	**Poly-Silicon**	**Poly-Silicon**	**Metal/Poly-Si**	**Metal/Poly-Si**
Is	*Upper electrode*						**1.Metal/Poly-Si 2. Metal**	**1.Metal/Poly-Si 2. Metal**
Was	*Capacitor Structure / dielectric*	**Silicon-Insulator-Silicon / NO**			**Silicon-Insulator-Silicon / High-κ**		**Metal Silicon-Insulator-Silicon / High-κ**	
Is	*Capacitor Structure / dielectric*						**1. Metal Silicon-Insulator-Silicon / High-κ 2. Metal-Insulator-Silicon/High-k**	



2003 Projects

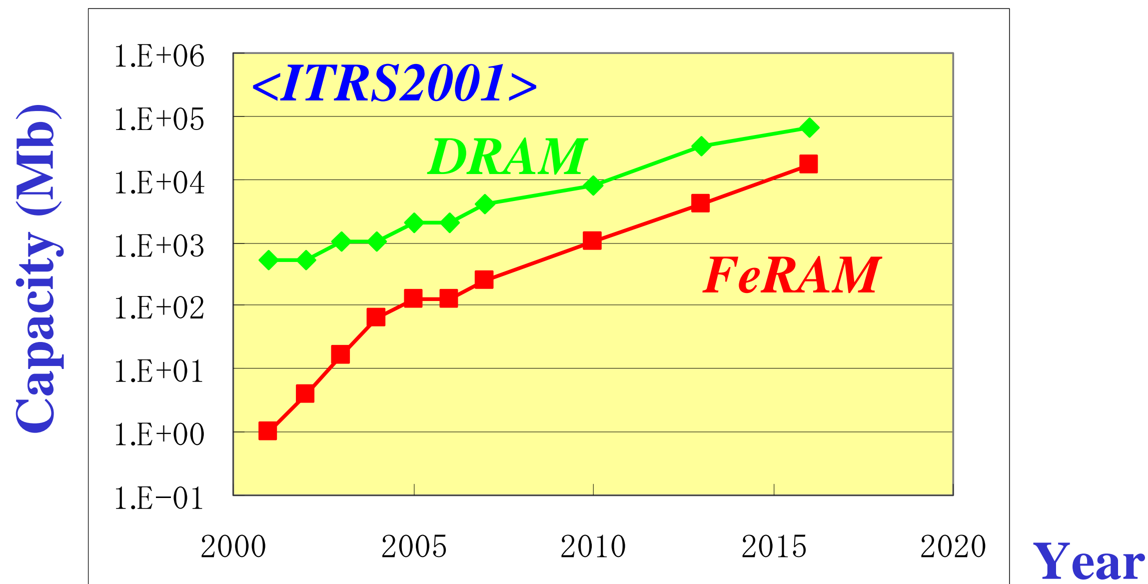
Concentrate on DRAM trench capacitor potential solutions

Flash Memory - 2002 Updates and 2003 Projects

- **2002 Updates**
  - **One-year roadmap pull-in with consequent changes to all requirements**
  - **Updated NAND tunnel and interpoly dielectric layers**
- **2003 Projects**
  - **Concentrate on Flash potential solutions**
  - **Red walls loom on tunnel- and interpoly- EOT**
  - **Other Projects TBD**
- **The Flash TWG is eagerly looking for US and Japan participants for 2003 projects. Interested parties should leave their business cards at the FEP poster boards.**

FeRAM - 2002 Updates and 2003 Projects

- **2002 Updates**
  - **No updates**
- **2003 Projects**
  - **Concentrate on developing requirements and potential solutions needed for continued scaling of the FeRAM storage cell**



2002 Update Summary

- **Update Starting Materials Cell Keys for supplier capability and metrology readiness**
- **Lg is slowed by one year for LSTP (Thin Film Table)**
- **Added NMOS drain extension doping requirements**
- **DRAM Trench capacitor structures changed**
- **Flash roadmap accelerated by one year**
- **Error correction and footnote text editing**

2003 Program Summary 1

- **Requirements and potential solutions for next generation silicon substrate (450mm?)**
- **Consider Site Flatness Model proposed by JEITA**
- **Update SOI requirements and potential solutions, including (Strained) Si:Ge on buried oxide**
- **Update Starting Substrate Defect Densities to reflect updated DRAM and MPU active areas**
- **Surface Prep: Review drivers for critical metals**

2003 Program Summary 2

- Update gate leakage models and requirements forecasts
- Update MOSFET source/drain resistance models and forecasts
- Update polysilicon depletion models and doping forecasts
- Update CD etch requirements based on new variance budget allocation between litho and etch
- STI etch and fill requirements and potential solutions
- Update memory cell scaling and potential solutions
- Review and develop FEP requirements for Emerging Memory and Logic Devices