

# **Design ITWG**

## **December 2002 Update**

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**International Technology Roadmap for Semiconductors**

*4 December 2002, ITRS 2002 Update Conference*

# Design ITWG Contributions to ITRS

- System Drivers Chapter
  - Defines IC products that drive manufacturing and design technologies
  - ORTCs + System Drivers = framework for technology requirements
  - Three System Driver classes
    - MPU
    - SOC (Low-Power, High-Performance, Mixed-Technology)
    - Mixed-Signal
- Design Chapter
  - Design cost and productivity models
  - Five technology areas: design process, system-level design, logical/physical/circuit design, design verification, design test
  - Cross-cutting challenges: productivity, power, manufacturing integration, interference, error-tolerance
- ORTC support
  - Frequency, Power, Density models



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# Big Picture

- Message: Cost of Design threatens continuation of the semiconductor roadmap
  - Design cost model
  - Challenges are now Crises
- Strengthen bridge from semiconductors to applications, software, architectures
  - Hertz and bits are not the same as efficiency and utility
  - System Drivers chapter, with productivity and power foci
- Strengthen bridges among ITRS technologies
  - “Shared red bricks” can be solved (or, worked-around) more cost-effectively
  - “Manufacturing Integration” cross-cutting challenge
  - “Living ITRS” framework to promote consistency validation



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# “Design-Manufacturing Integration”

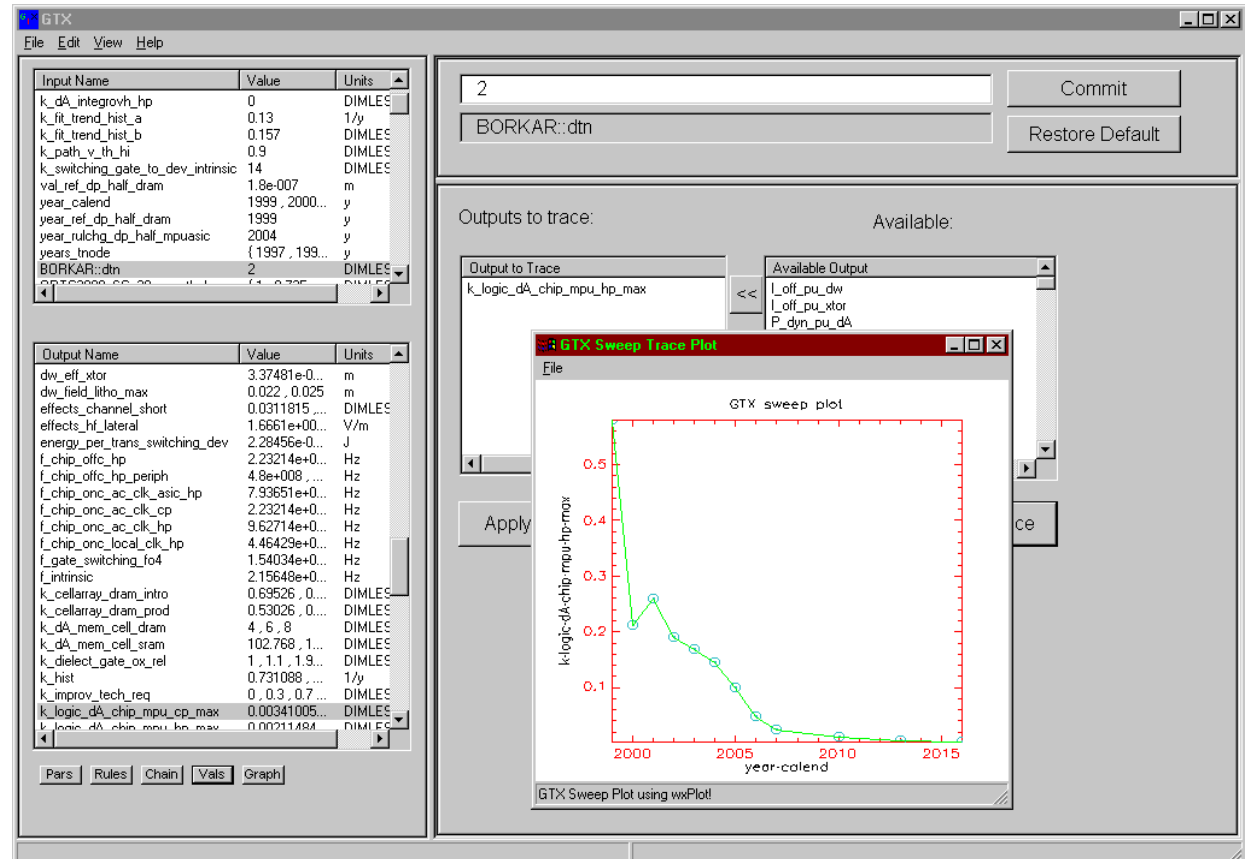
- 2001 ITRS Design Chapter: “Manufacturing Integration” = one of five Cross-Cutting Challenges
- Goal: share red bricks with other ITRS technologies
  - Lithography CD variability requirement → new Design techniques that can better handle variability
  - Mask data volume requirement → solved by Design-Mfg interfaces and flows that pass functional requirements, verification knowledge to mask writing and inspection
  - ATE cost and speed red bricks → solved by DFT, BIST/BOST techniques for high-speed I/O, signal integrity, analog/MS
  - Does “X initiative” have as much impact as copper?



# “Living ITRS” Framework

- “Living roadmap”: internally consistent, transparent models as basis of ITRS predictions

- ORTCs: Models for layout density, system clock speed, total system power in various drivers, circuit fabrics
- Visualization tool (at Sematech website) for capture, exploration of ITRS models under alternative scenarios



# Core Messages

- Design Technology = interface from semiconductor industry to systems and applications markets
- Cost of Design is a key threat to semiconductor productivity
- “Shared Red Bricks”
  - Framework for roadmapping that allows principled allocation of R&D resources across ITRS technologies
  - Role of Design Technology in reducing cost of, or enabling workarounds for, near-term red bricks
- “Living ITRS”



# SYSTEM DRIVERS CHAPTER



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# Reorganized System Drivers

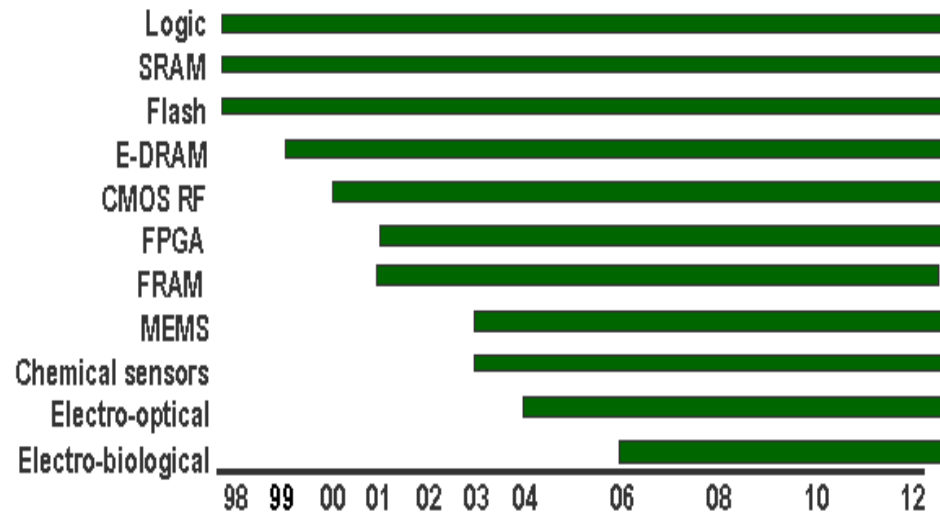
## Chapter

- Change to SOC-centered organization
- SOC = unifying context for various blocks and fabrics
  - Processor
  - Mixed-Signal
  - Embedded memory (eSRAM, eDRAM, eFlash)
    - Traditional metrics: bitcell area, access time, power, ...
    - Cost, amenability to integration, requirements from applications
    - Yield, testability, reliability
    - Future memory types (MRAM, FeRAM, ...)
  - Embedded DSP and MCU
    - Addition to MPU (processor) discussion
    - Discussion of architecture, figures of merit
- Target = 2003



# SOC-MT Integration Roadmap

- System Drivers Figure 10
  - FRAM in production on standard CMOS process
  - Could not find instances of MEMS, Chemical Sensors in production on standard CMOS process
  - 2002 update: → pushed out one year



- Economic constraints and system-in-package integration alternatives
  - Very large set of issues (testability and test cost, die cost modeling, performance/cost tradeoffs, etc.), possible for 2003 renewal



# SOC-LP

- System Drivers Table 11 match with Table 36 (PIDS)
  - Target = 2003
- LOP/LSTP subthreshold currents (Tables 11, 36) too low
  - Too optimistic, not achievable even today
  - 2002: already a crisis for low-power portable systems
  - Cross-ITWG issue with PIDS ITWG
  - Target = 2003



# SOC-LP PDA Model

- Table 10 (functional requirements of SOC-LP model and technology baseline) updated in 2003
- Mixed-signal content (e.g., Bluetooth)
  - Affects die area usage, power budget, ATE and test strategy, etc.
- Model parameters under reconsideration
  - Performance and die size
  - Device and memory composition
    - % logic vs. memory, % HP vs. LP, % SRAM vs. eDRAM
  - Target = March 2003, validated with Dataquest/SI2 study
- Battery technology
  - 7-8%/year historical improvement to be used in Table 12
  - Potential 10x from fuel cells



# Other Possibilities

- Impact of cost drivers
  - Low metal layer count (low mask count) technology
  - Mixed-signal integration
  - Cf. dynamics of FPGA, microcontroller markets
- Roadmap for off-chip signaling bandwidth
  - Part of SOC-HP (high-end, e.g., core networking)
  - Related to package pin count, tester roadmaps
    - ESD protection limits and impact on signaling speed
  - Shared by A&P, Test, and Design



# DESIGN CHAPTER



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# Revised Design Chapter

- Existing content better highlighted by chapter reorganization
  - All tables of Difficult Challenges written so that issues are specific to a driver class (AMS, MPU, SOC)
  - Prototype = Table 16 in 2001 ITRS (Design Verification)
- New material
  - More standalone analog, circuits content
  - Canonical design flow context
  - Soft-error rate
- Improvements to existing material
  - Design cost model
  - Design system architecture



# Design Flow, Cost, and System Architecture

- Canonical design flow needed to provide context for detailed technology discussions
  - Defined by STRJ-WG1
  - Also serves as grounding for design cost analysis
- Design cost model refinement
  - Clarify model description
  - Calibrate memory content of constant design cost SOC (higher than observed industry data)
- Design system architecture
  - Super-exponential complexities of the design problem require more attention to the architecture of future design systems
  - Issues: infrastructure, design environment, etc.



# Soft-Error Rate

- Figures of merit and roadmap for SER
- Both memory (eSRAM, eDRAM) and logic
- Technology integration implications
  - Flip-chip packaging, SOI
- Device architecture implications
- Design implications
  - Error-detection, error-correction
- Target = 2003



# Example Cross-ITWG Interactions

- Interconnect: BEOL Architecture Optimization
  - “Is low-k (e.g., reduction from 3.0 to 2.8) worth it?” “If we stop at 2.0, will the world end?”
  - “What is the optimal interconnect stack that satisfies via and (damascene copper) metal aspect ratio constraints?”
  - “What is the variability (copper dishing and erosion, or poly CD control) that designers can tolerate?”
  - “What ground rules (poly half-pitch, contacted M1 pitch, ...) comprise the tightest limiters on layout density?”
- Assembly and Packaging, Factory Integration, Test
  - “What are limits on off-chip signaling speed imposed by ESD protection?”
- Assembly and Packaging, Environmental Safety and Health
  - “What are high-performance (MPU) system power requirements?”
  - = “resource reduction requirement” for environmental safety



# SUMMARY



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# Summary

- System Drivers Chapter
  - New material
    - Embedded memory
    - Embedded DSP, MCU
  - Improvements to existing material
    - SOC-MT integration timeline
    - SOC-LP device and system parameters
    - “SOC-centric” chapter reorganization
- Design Chapter
  - New material
    - Analog and circuits content
    - Canonical design flow context
    - SEU discussion
  - Improvements to existing material
    - Design cost model refinement
    - Design system architecture

