Errata

January 16, 2003

This posting of *The International Technology Roadmap for Semiconductors, 2002 Update,* contains the following corrections:

Front End Processes

Table 48 Front End Processes Difficult Challenges, line item for Critical dimension and effective channel length (L_{eff}) control was corrected to delete ~15% 3σ

Is	Critical dimension and effective channel length (L_{eff}) control	Control of self-aligned doping processes and thermal activation budgets to achieve ~~~15% 3σ~~ L_{eff} contro

Table 50a and b Surface Preparation Technology Requirements*—Near-term and long-term lines for wafer edge exclusion was corrected to include the updated wafer edge exclusion and particles per wafer

Was	*Wafer edge exclusion (mm)*	3	3	1	1	1	1	1	*D ½, M*
Is	*Wafer edge exclusion (mm)*	3	3	2	2	2	2	2	*D ½, M*

Was	Particles (#/wafer) [C]	63	94	60	83	48	66	39	*D ½*
Is	Particles (#/wafer) [C]	62	92	59	82	47	65	38	*D ½*

Table 50b Surface Preparation Technology Requirements*—Long-term

Was	*Wafer edge exclusion (mm)*	1	1	1	*D ½, M*
Is	*Wafer edge exclusion (mm)*	2	2	2	*D ½, M*

Notes for Tables 50a and b were corrected to delete "or bits" in note (B)

Is	*(B) $Y=0.99=exp[-D_pR_pA_{eff}]$. For DRAM, $A_{eff}=2.5F^2T+(1-aF^2T/A_{chip})*0.6A_{chip}$. Where F is the minimum feature size (CD), a is the cell fill factor (see Table 52), T is the number of transistors ~~or bits~~ per chip (see Table 1c) and A_{chip} is the chip size (see Table 1c). For MPUs, $A_{eff}=aT(GL)^2$, where GL is the gate length and a and T are specified for MPUs. The kill factor, R_p, is taken as 0.2. $D_p=-ln(0.99)/[R_pA_{eff}]$. If a different critical Particle size (Dx) is used for measurement purposes then D_p should be adjusted by $(Dx/.5CD)^2$. Note that the year-to-year value for D_p does not always decrease because D_p is not only inversely proportional to T, which increases each year, but is also inversely proportional to a and F, which are decreasing year-to-year, and A_{chip} which moves up and down.*

Table 51a and b Thermal & Thin Film, Doping and Etching Technology Requirements—Near-term and long-term were corrected to include low operating power and data change and add low standby power data

Is	*Physical gate length low operating power (LOP) (nm)*	90	75	65	53	45	37	32	*Low Power*
Add	*Physical gate length low standby power (LSTP) (nm)*	100	90	75	65	53	45	37	*Low Power*
	Equivalent physical oxide thickness for low operating power Tox (nm) [A]	2.0-24	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4	*LOP*

Table 51b Thermal & Thin Film, Doping and Etching Technology Requirements—Long-term

Is	*Physical gate length low operating power (LOP) (nm)*	22	16	11	*Low Power*
Add	*Physical gate length low standby power (LSTP) (nm)*	28	20	16	*Low Power*