TEST

Table 19 Test Difficult Challenges

Five Difficult Challenge ≥ 65 nm , Through 2007	*Summary of Issues*
High Speed Device Interfaces	A major roadblock will be the need for high-frequency, high pin-count probes and test sockets; research and development is urgently required to enable cost effective solutions with reduced parasitic impedance. High speed serial interface speed and port count trends will continue to drive high speed analog source/capture and jitter analysis instrument capability for characterization. DFT/DFM techniques must be developed for manufacturing. Device interface circuitry must not degrade equipment bandwidth and accuracy, or introduce noise; especially for high-frequency differential I/O and analog circuits.
Highly Integrated Designs	Highly structured DFT approaches are required to enable test access to embedded cores. Individual cores require special attention when using DFT and BIST to enable test. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever increasing instrument capability trends. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits. DFT must enable test reuse for reusable design cores to reduce test development time for highly complex designs.
Reliability Screens	Existing methodologies are limited (burn-in versus thermal runaway, IDDQ versus background current increases). Research is required to identify novel infant mortality defect acceleration stress conditions
Manufacturing Test Cost	Test cell throughput enhancements are needed to reduce manufacturing test cost. Opportunities include massively parallel test, wafer-level test, wafer-level burn-in, and others. Challenges include device interfacing/contacting, power and thermal management. Device test needs must be managed through DFT to enable low cost manufacturing test solutions; including reduced pin count test, equipment reuse, and reduced test time. Automatic test program generators are needed to reduce test development time. Test standards are required to enable test content reuse and manufacturing agility.
Modeling and Simulation	Logic and timing accurate simulation of the ATE, device interface, and DUT is needed to enable pre-silicon test development and minimize costly post-silicon test content development/debug on expensive ATE. High performance digital and analog I/O and power requirements require significant improvements to test environment simulation capability to ensure signal accuracy and power quality at the die. Equipment suppliers must provide accurate simulation models for pin electronics, power supplies, and device interfaces to enable interface design.

Table 19 Test Difficult Challenges (continued)

Five Difficult Challenges <65 nm, Beyond 2007	
DUT to ATE interface	Probing capability for optical and other disruptive technologies. Support for massively parallel test - including full wafer contacting. Decreasing die size and increasing circuit density are driving dramatic increases in die thermal density. This problem is further magnified by the desire to enable parallel test to maximize manufacturing throughput. New thermal control techniques will be needed for wafer probe and component test. DFT to enable test of device pins not contacted by the interface and test equipment.
Test Methodologies	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years). New test methods for control and observation are needed. Tests will need to be developed utilizing the design hierarchy. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever increasing instrument capability trends. Logic BIST techniques must evolve to support new fault models, failure analysis, and deterministic test. EDA tools for DFT insertion must support DFT selection with considerations for functionality, coverage, cost, circuit performance and ATPG performance.
Defect Analysis	Defect types and behavior will continue to evolve with advances in fabrication process technology. Fundamental research in existing and novel fault models to address emerging defects will be required. Significant advances in EDA tools for ATPG capacity and performance for advanced fault models and DFT insertion are required to improve efficiency and reduce design complexities associated with test.
Failure analysis.	Realtime analysis of defects in multi-layer metal processes are needed. Failure analysis methods analog devices must be developed and automated. Transition from a destructive physical inspection process to a primarily non-destructive diagnostic capability. Characterization capabilities must identify, locate, and distinguish individual defect types.
Disruptive device technologies	Develop new test methods for MEMS and sensors. Develop new fault models for advanced/disruptive transistor structures.

Table 23a High Frequency Serial Communications Test Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	High–performance-level serial transceivers							
	Serial data rate (Gbits/s)	**10**	**10**	**40**	**40**	**40**	**40**	**40**
	Maximum reference clock speed (MHz)	**667**	**667**	**2500**	**2500**	**2500**	**2500**	**2500**
	High-integration-level backplane and computer I/O							
	Serial data rate (Gbits/s) Production	**2.5**	**3.125**	**3.125**	**10**	**10**	**40**	**40**
Was	Introduction	**3.125**	**—**	**10**	**—**	**40**	**—**	**—**
Is	Introduction	**3.125**	**—**	**10**	**—**	**40**	**—**	**—**
	Maximum port count at Production frequencies	**20**	**100**	**200**	**100**	**200**	**100**	**200**
	at Introduction frequencies	**—**	**—**	**20**	**—**	**20**	**—**	**—**
	Maximum reference clock speed (MHz) Production	**166**	**166**	**166**	**667**	**667**	**2500**	**2500**
	Introduction	**—**	**—**	**667**	**—**	**2500**	**—**	**—**

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

*Table 28 DFT-BIST Device Test Requirements—Near-term***

	Year of Production	2001	2002	2003	2004	2005	2006	2007	Driver
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65	
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65	
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35	
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25	
	Number of parallel sites	32	32	64	64	128	128	128	Cost
Was	Scan data volume(Giga-pin-vectors available per site)	6	6	12	12	16	16	16	Logic Density
Is	Scan data volume(Giga-pin-vectors available per site)	6	6	12	12	16	16	32	
Was	Scan pin (available per site / system)	256/1K	256/1K	256/2K	256/2K	256/4K	256/4K	256/4K	Logic Density
Is	Scan pin (available per site / system)	256/1K	256/1K	384/2K	384/2K	512/4K	512/4K	512/4K	
	Scan vector rate (MT or MHz)	50	100	100	200	200	200	200	Test Time
	"Full function" pin (available per site / system)	128/256	128/256	128/512	128/512	128/512	128/512	128/512	Test Time
	Functional vector depth (M-Vectors)	16	16	16	16	16	16	16	Logic Density
	Functional data rate (MHz)	100	100	100	200	200	200	200	Test Time
	"Reduced function" pin (available per site / system)(DC only)	3K/4K	3K/4K	3K/4K	4K/5K	4K/5K	5K/6K	5K/6K	I/O Density
	Clock pins (available per site / system)	4/32	4/32	4/64	4/64	4/128	4/128	4/128	Clock Domains
	Clock frequency (MHz)	200	200	400	400	400	800	800	On-chip Clock Rate
	Power supplies (available per site / system)	8/32	8/32	8/64	8/64	8/128	8/128	8/128	Logic Density
	Support for options								SoC
	High-speed clock (differential pairs)	yes	yes	yes	yes	yes	yes	yes	
	Signature compression	yes	yes	yes	yes	yes	yes	yes	
	Algorithmic pattern generation	yes	yes	yes	yes	yes	yes	yes	
	Low-frequency source and digitizer	yes	yes	yes	yes	yes	yes	yes	
	High-frequency source and digitizer	yes	yes	yes	yes	yes	yes	yes	
	Time measurement unit	yes	yes	yes	yes	yes	yes	yes	
	ADC/DAC	yes	yes	yes	yes	yes	yes	yes	
	RF source	no	no	yes	yes	yes	yes	yes	
	High power	yes	yes	yes	yes	yes	yes	yes	
	IDDQ	yes	yes	yes	yes	yes	yes	yes	

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

Definitions for Table 28:

	Parallel Sites—Parallel testing of devices is a common technique for reducing the effective cost of test per device by testing multiple devices with a single tester. The number of devices that can be tested in parallel will be necessarily limited by the tester's available physical resources, however there should be no "logical" limit imposed by the hardware or software architecture. A common concern with these tables in the past has been the total number of pins that seem to be indicated by multiplying all of the numbers together, however this is not the intent. The total number of pins available on a given tester should be consistent with the current state-of-the-art for pin densities.
	Scan Data Volume—The total number of bits shifted into the scan input pins plus the total number of bits shifted out of scan output pins. It is the total number of scan-able elements in a device multiplied by the total number of scan-loads plus the scan-unloads. A single bit shifted into a single device pin or shifted out of a single device pin can be defined as pin-vector (a tester architecture neutral unit).
Was	*Scan Pin*—The maximum number of scan input pins and scan output pins. This number does not necessarily include the pins required for scan control.
Is	*Scan Pin*—The maximum number of scan input pins **plus** scan output pins. This number does not necessarily include the pins required for scan control.
	Scan Vector Rate—The maximum shift rate for scan data input pins and scan data output pins (expressed in MegaTransfers per second (MT)).
	"Full Function" Pin—Full Function pins are backed by drive and receive resources containing the full functionality of a traditional ATE system pin. These resources may include, but are not necessarily limited to, precision timing accuracy, flexible waveform capability, high vector rates, programmable drive/receive thresholds, parametric measurement capability, etc. These "Full Function" pins are used to test the DUT via a traditional ATE approach utilizing device primary I/O pins which may include, but are not limited to the following functions: clock, input, output, bi-directional, and reference level bias (fixed state controlled by ATE pin electronics). In addition, the full function pins should be capable of scan (either within the limits of "Full Function" pin memory depth or with access to the scan memory).
	Functional Vector Depth—The total number of vectors required to test a particular device. In this context, it refers to the total number of individual states (e.g., "0," "1," "H," "L," "X," "Z," etc.) applied to or received from a single device pin.
	Functional Data Rate – The maximum rate of application of vectors to the data pins of the device.
	"Reduced Function" Pin—Reduced Function pins are backed by low-cost resources containing limited digital drive/receive capability (e.g. static vectors are vectors that remain static for the duration of a particular test or subtest), no waveform capability, very little vector depth, etc. These pins will typically have programmable drive/receive thresholds, and parametric measurement capability.
	Clock Pin—These single-ended clock pins function at higher frequencies and higher accuracies than the scan and functional data pins. These clocks are used for functional testing at the functional data rate, as well as, AC scan (shift slow – sample fast) and BIST, to facilitate high performance testing on DFT testers.
	Clock Frequency—The maximum frequency attainable from the standard clock source. The accuracy and skew for the clock pins should be maintained to less than or equal to 8% of the minimum clock period and the jitter should be less than or equal to 1.5% of the minimum clock period.
	Power Supplies—ATE device power supplies provide programmable voltage (or current) levels during testing. The most typical application is to apply voltage and current to a device's primary power connections such as V_{cc} or V_{dd}. Other uses include reference voltage sources for device pins, termination voltages for external loads, and current sourcing during test. Device power supplies may be used in forcing either current or voltage while measuring the resulting voltage or current. Common feature include programmable clamps, measurement trigger/capture controlled by the tester's pattern generator, and switch-able output voltage ranges controlled by the pattern generator. Supplies should be gang-able for flexibility.
	Support for Options—There will always be a need to support options. This is driven by the need to support legacy devices in the Functional-to-Structural transition phase, as well as, for devices with mature DFT and some mixed-signal or extended performance requirements. The remaining line items in this table try to predict the need and performance requirements of some of the more typical of these options in the future. There are a number of analog options – these have been specifically identified, though this may not be a comprehensive list.
	High-Speed Clock Pin—The high-speed clock pins function at higher frequencies and higher accuracies than the "standard" clock source. The high-speed clocks should support both single-ended operation and differential clock pairs. The maximum frequency required for this clock option is 800MHz through 2003, rising to 1.4GHz in 2004. The accuracy and skew for the high frequency clock pins should be maintained to less than or equal to 8% of the minimum clock period and the jitter should be less than or equal to 1.5% of the minimum clock period.

Definitions for Table 28 (continued):

Was	*Signature Compression*—Integrating Linear Feedback Shift Registers (LFSRs) with the scan channels on the DFT tester can dramatically reduce scan data volume and test time. Pseudo Random Pattern Generators (PRPGs) can be used to minimize the amount of scan-in stimuli that need to be stored in the scan buffer. Single Input Signature Registers (SISRs) can be used to compress scan-out measures. The PRPGs and SISRs should be integrated with the scan channels such that an individual scan cycle can interact with either its LFSR / SISR or scan channel. The LFSRs / SISRs should have programmable polynomials. The LFSRs/ SISRs should be capable of having their states seeded, reset, and observed under pattern op-code control and from states stored in pattern memory.
Is	*Stimulus/Response Compression*—Integrating Linear Feedback Shift Registers (LFSRs) **as Pseudo Random Pattern Generators (PRPGs) or as Single Input Signature Registers (SISRs), on-chip, or with the scan channels** on the DFT tester can dramatically reduce scan data volume and test time **by minimizing the amount of test data that needs to be stored in the scan buffer**. ~~Single Input Signature Registers (SISRs) can be used to compress scan-out measures. The PRPGs and SISRs should be integrated with the scan channels such that an individual scan cycle can interact with either its LFSR / SISR or scan channel.~~ The LFSRs / SISRs should have programmable polynomials. The LFSRs/ SISRs should be capable of having their states seeded, reset, and observed under pattern op-code control and from states stored in pattern memory.
	Algorithmic Pattern Generation—Memory pattern sequences are generally repetitive and can, therefore, be generated algorithmically. Algorithmic Pattern Generator functionality should be integrated with other tester pattern sources to allow operation concurrently with stored stimulus/response test patterns.
Was	*Low Frequency Source/Digitizer*—The ability to generate and digitize a differential analog waveform, such as a ramp or sine wave. Generally, 18-bit resolution up to 100KHz.
Is	*Low Frequency Source/Digitizer*—The ability to generate and digitize ~~a differential~~ analog waveforms, such as a ramp or sine wave. Generally, 18-bit resolution up to **350K samples/second**.
Was	*High Frequency Source/Digitizer*—The ability to generate and digitize a differential analog waveform, such as a ramp or sine wave. Generally, 12-bit resolution up to 10MHz.
Is	*High Frequency Source/Digitizer*—The ability to generate and digitize ~~a differential~~ analog waveform, such as a ramp or sine wave. Generally, 12-bit resolution up to **30M samples/second.**
Was	*Time Measurement*—Ability to measure a time interval or frequency.
Is	*Time Measurement*—Ability to measure a time interval or frequency. **The instrument should allow taking the measurement at the occurrence of an enabling event.**
	RF Source—As Radio Frequency functions find their way onto more and more SoCs and appropriate DFT sampling methodologies are developed for RF, there will be a need for external resources to generate clean, high frequency sine waves. The frequency requirements of these resource will be in the 100MHz to 6GHz range.
	High Power—Some devices consume very high power (>75W), during tests. High-current device power supplies must deliver accurate voltage and respond quickly to load changes (on the order of 1–2µs). In addition, significant current is applied through the tooling fixture and contactors or probe needles. There may be 1000s of device power pins in extremely tight physical density. The power supply must be capable of performing integrity tests that detect discontinuities such as power shorts to prevent damage to expensive test fixtures. In general, flexible user control of fast-acting safety/error, clamping, and shutdown hardware features becomes more important in high power delivery.

Table 30a Commodity Flash Memory Test Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*Driver*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	
	MPU Printed Gate Length(nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	
	Device Characteristics								
Was	Density (megabits): volume production	64	128	128	256	256	512	512	
Is	Density (megabits): volume production	64	128	256	256	512	512	1024	
Was	Density (megabits): lead density	512	512	1024	1024	2048	4096	4096	
Is	Density (megabits): lead density	512	1024	1024	2048	4096	4096	8192	
	Data width (bits)	32	32	32	32	32	32	32	
	Simultaneously tested devices (wafer test)	64	64	64	128	128	128	128	
Was	Simultaneously tested devices (package test)	64	64	64	128	128	128	128	
Is	Simultaneously tested devices (package test)	64	128	128	128	128	256	256	
	Power Supplies								
Was	Power supply voltage range	0.6–5.5	0.6–5.5	0.6–5.5	0.6–3.3	0.6–3.3	0.6–3.3	0.6–3.3	
Is	Power supply voltage range	0.6–5.5	1.0-5.5	1.0-5.5	1.0-5.5	1.0-5.5	0.6–3.3	0.6–3.3	
	Power supply accuracy (% of programmed value)	5	5	5	5	5	5	5	
	Maximum current (MA)	200	200	300	300	300	300	300	
Was	Programming power supply voltage range (V)	0.6–10.0	0.6–10.0	0.6–10.0	0.6–10.0	0.6–10.0	0.6–10.0	0.6–8.0	
Is	Programming power supply voltage range (V)	0.6–10.0	1.0-12.0	1.0-12.0	1.0-12.0	0.6–10.0	0.6–10.0	0.6–8.0	
	Pattern Generator								
	Tester channels per test site [1]	64	64	64	64	64	64	64	
	Vector depth (millions)	1	1	1	1	1	1	1	
	Scan vector depth (millions) [2]	2	4	4	4	4	4	4	*On-chip or multi-chip logic*
	APG addresses [3]	48	48	48	48	48	48	48	
	Timing								
	Maximum data rate (MHz)	80	100	125	133	166	166	166	
	Accuracy OTA (ns)	0.75	0.6	0.6	0.5	0.5	0.5	0.5	
	Cost								
	Tester cost per pin ($) [4] [5]	1000	950	903	857	815	774	735	
	Reliability								
	MTBF (hours) [6]	3000	3150	3308	3473	3647	3829	4020	
	MTTR (hours)	1	1	1	1	1	1	0.5	
	Availability (%)	99	99	99.5	99.5	99.5	99.5	99.5	
	Setup time (hours)	0.4	0.4	0.3	0.3	0.2	0.2	0.2	

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

Table 30b Commodity Flash Memory Test Requirements—Long-term

	Year of Production	2010	2013	2016	Driver
	DRAM ½ Pitch (nm)	45	32	22	
	MPU / ASIC ½ Pitch (nm)	45	32	22	
	MPU Printed Gate Length (nm)	25	18	13	
	MPU Physical Gate Length (nm)	18	13	9	
	Device Characteristics				
	Density (megabits): volume production	2048	4096	8192	
	Density (megabits): lead density	16384	65536	131072	
	Data width (bits)	32	32	32	
Was	Simultaneously tested devices (wafer test)	256	256	256	
Is	Simultaneously tested devices (wafer test)	256	512	512	
	Simultaneously tested devices (package test)	256	256	256	
	Power Supplies				
	Power supply voltage range	0.6–3.3	0.6–3.3	0.6–3.3	
	Power supply accuracy (% of programmed value)	5	5	5	
	Maximum current (MA)	300	300	300	
	Programming power supply voltage range (V)	0.6–8.0	0.6–8.0	0.6–8.0	
	Pattern Generator				
	Tester channels per test site [1]	72	72	72	
	Vector depth (millions)	2	2	2	
	Scan vector depth (millions) [2]	8	8	8	*On-chip or multi-chip logic*
	APG addresses [3]	48	48	48	
	Timing				
	Maximum data rate (MHz)	200	250	300	
	Accuracy OTA (ns)	0.3	0.2	0.1	
	Cost				
	Tester cost per pin ($) [4] [5]	630	540	463	
	Reliability				
	MTBF (hours) [6]	4654	5388	6237	
	MTTR (hours)	0.5	0.5	0.5	
	Availability (%)	99.5	99.5	99.5	
	Setup time (hours)	0.2	0.2	0.2	

White–Manufacturable Solutions Exist, and Are Being Optimized
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Red–Manufacturable Solutions are NOT Known

Table 32a Burn-in Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	High Performance ASIC							
	Clock input frequency (MHz)	400	400	400	400	400	400	400
	Off-chip data frequency (MHz)	25	50	50	75	75	75	75
	Power supply voltage range (V)	0.7–4.0	0.7–4.0	0.7–3.3	0.7–2.5	0.5–2.5	0.5–2.5	0.5–2.5
Was	Power dissipation (W per DUT)	130	140	150	150	200	200	200
Is	Power dissipation (W per DUT)	30	40	50	75	100	150	200
	Maximum number of signal I/O	384	384	384	384	384	384	384
	High Performance Microprocessor							
Was	Clock input frequency (MHz)	150	200	200	250	250	250	250
Is	Clock input frequency (MHz)	150	200	200	250	400	400	400
	Off-chip data frequency (MHz)	33	75	75	75	75	75	75
Was	Power supply voltage range (V)	0.7–4.0	0.7–3.5	0.7–3.5	0.5–3.5	0.5–3.5	0.5–3.5	0.5–3.5
Is	Power supply voltage range (V)	0.7–4.0	0.7–3.5	0.7–3.5	0.5–3.5	0.5–2.5	0.5–2.5	0.5–2.5
Was	Power dissipation (W per DUT)	150	200	200	250	300	300	300
Is	Power dissipation (W per DUT)	150	200	200	250	600	600	600
Was	Maximum current (A)	75	150	150	300	300	300	300
Is	Maximum current (A)	75	150	150	300	400	450	450
	Maximum number of signal I/O	128	128	128	128	128	128	128
	Low-End Microcontroller							
	Clock frequency (MHz)	25	100	200	300	400	400	400
	Off-chip data frequency (MHz)	25	40	50	60	75	75	75
	Power supply voltage range (V)	0.7–12.0	0.7–12.0	0.7–12.0	0.7–10.0	0.7–10.0	0.7–10.0	0.7–10.0
	Power dissipation (W per DUT)	3	5	5	10	10	10	10
	Maximum number of signal I/O	32	32	32	32	32	32	32
	Mixed-Signal							
	Clock input frequency (MHz)	150	200	200	250	250	250	250
	Off-chip data frequency (MHz)	33	75	75	75	75	75	75
	Power supply voltage range (V)	0.7–65.0	0.7–65.0	0.7–100	0.7–100	0.5–500	0.5–500	0.5–500
	Power dissipation (W per DUT)	50	50	75	75	150	150	150
	Maximum current (A)	20	20	20	20	20	20	20
	Maximum number of signal I/O	128	128	128	128	128	128	128
	Analog signal peak-to-peak voltage range (V)	±10V	±10V	±10V	±10V	±10V	±10V	±10V
	Commodity Memory							
	Clock input frequency (MHz)	400	400	400	400	400	400	400
	Off-chip data frequency (MHz)	30	30	30	50	50	50	50
	Power supply voltage range (V)	0.6–6.0	0.6–6.0	0.6–6.0	0.6–4.0	0.6–4.0	0.6–4.0	0.6–4.0
	Programming power supply voltage range (V)	0.6–10	0.6–10	0.6–10	0.6–10	0.6–10	0.6–10	0.6–8
	Power dissipation (W per DUT)	2	5	10	15	20	20	20
	Maximum number of signal I/O	18	36	36	72	72	72	72
	DFT / BIST Requirements							
	Scan pin count (per DUT)	128	128	128	128	128	128	128
	Scan vector memory depth (megavectors)	64	128	256	256	256	256	256
	Scan vector frequency (MHz)	33	75	75	75	75	75	75

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

Table 32b Burn-in Requirements—Long-term

	Year of Production	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*45*	*32*	*22*
	MPU Printed Gate Length (nm)	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*18*	*13*	*9*
	High Performance ASIC			
	Clock input frequency (MHz)	**400**	**400**	**400**
	Off-chip data frequency (MHz)	**75**	**75**	**75**
	Power supply voltage range (V)	**0.5–2.5**	**0.5–2.5**	**0.4–2.5**
	Power dissipation (W per DUT)	**200**	**225**	**250**
	Maximum number of signal I/O	**384**	**384**	**384**
	High Performance Microprocessor			
Was	Clock input frequency (MHz)	**250**	**250**	**250**
Is	Clock input frequency (MHz)	**400**	**400**	**400**
	Off-chip data frequency (MHz)	**75**	**75**	**75**
Was	Power supply voltage range (V)	**0.5–3.0**	**0.5–2.5**	**0.5–2.5**
Is	Power supply voltage range (V)	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**
Was	Power dissipation (W per DUT)	**300**	**300**	**300**
Is	Power dissipation (W per DUT)	**600**	**600**	**600**
Was	Maximum current (A)	**300**	**300**	**300**
Is	Maximum current (A)	**450**	**450**	**450**
	Maximum number of signal I/O	**128**	**128**	**128**
	Low-End Microcontroller			
	Clock frequency (MHz)	**400**	**400**	**400**
	Off-chip data frequency (MHz)	**75**	**75**	**75**
	Power supply voltage range (V)	**0.5–10**	**0.5–10**	**0.5–10**
	Power dissipation (W per DUT)	**20**	**20**	**20**
	Maximum number of signal I/O	**32**	**32**	**32**
	Mixed-Signal			
	Clock input frequency (MHz)	**250**	**250**	**250**
	Off-chip data frequency (MHz)	**75**	**75**	**75**
	Power supply voltage range (V)	**0.5–500**	**0.5–1000**	**0.5–1000**
	Power dissipation (W per DUT)	**150**	**150**	**150**
	Maximum current (A)	**30**	**30**	**30**
	Maximum number of signal I/O	**128**	**128**	**128**
	Analog signal peak-to-peak voltage range (V)	**±10V**	**±10V**	**±10V**
	Commodity Memory			
	Clock input frequency (MHz)	**400**	**400**	**400**
	Off-chip data frequency (MHz)	**50**	**50**	**50**
	Power supply voltage range (V)	**0.5–4.0**	**0.5–4.0**	**0.5–4.0**
	Programming power supply voltage range (V)	**0.5–8.0**	**0.5–8.0**	**0.5–8.0**
	Power dissipation (W per DUT)	**20**	**20**	**20**
	Maximum number of signal I/O	**72**	**72**	**72**
	DFT / BIST Requirements			
	Scan pin count (per DUT)	**128**	**128**	**128**
	Scan vector memory depth (megavectors)	**256**	**256**	**256**
	Scan vector frequency (MHz)	**75**	**75**	**75**

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known