OVERALL TECHNOLOGY ROADMAP CHARACTERISTICS TABLES

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Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm) ††	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length) (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
ASIC/Low Power Printed Gate Length (nm) ††	**130**	**107**	**90**	**75**	**65**	**53**	**45**
ASIC/Low Power Physical Gate Length) (nm)	**90**	**75**	**65**	**53**	**45**	**37**	**32**

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term years

YEAR OF PRODUCTION	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm) ††	**25**	**18**	**13**
MPU Physical Gate Length) (nm)	**18**	**13**	**9**
ASIC/Low Power Printed Gate Length (nm) ††	**32**	**22**	**16**
ASIC/Low Power Physical Gate Length) (nm)	**22**	**16**	**11**

Notes for Tables 1a and 1b:

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "Physical" gate lengths may be reduced from the "as-printed" dimension. These "Physical" gate-length targets are driven by the need for maximum speed performance in logic Microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design ITWG Tables as needs that drive device design and process technology requirements.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms

.

Table 1c DRAM Production Product Generations and Chip Size Model—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Cell area factor [a]	**8**	**8**	**6**	**6**	**6**	**6**	**6**
Cell area [$Ca = af^2$] (μm^2)	**0.130**	**0.103**	**0.061**	**0.049**	**0.039**	**0.031**	**0.024**
Cell array area at production (% of chip size) §	**54.8%**	**55.3%**	**55.7%**	**56.1%**	**56.4%**	**56.7%**	**57.0%**
Generation at production §	**512M**	**512M**	**1G**	**1G**	**2G**	**2G**	**4G**
Functions per chip (Gbits)	**0.54**	**0.54**	**1.07**	**1.07**	**2.15**	**2.15**	**4.29**
Chip size at production (mm^2)§	**127**	**100**	**118**	**93**	**147**	**116**	**183**
Gbits/cm^2 at production §	**0.42**	**0.54**	**0.91**	**1.15**	**1.46**	**1.85**	**2.35**

Table 1d DRAM Production Product Generations and Chip Size Model—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Cell area factor [a]	**6**	**4**	**4**
Cell area [$Ca = af^2$] (μm^2)	**0.012**	**0.004**	**0.002**
Cell array area at production (% of chip size) §	**57.7%**	**58.1%**	**58.4%**
Generation at production §	**8G**	**32G**	**64G**
Functions per chip (Gbits)	**8.59**	**34.36**	**68.72**
Chip size at production (mm^2)§	**181**	**239**	**238**
Gbits/cm^2 at production §	**4.75**	**14.35**	**28.85**

Notes for Tables 1c and 1d:

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows:

1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

1. *at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and*
2. *at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).*

InTER-generation chip size growth rate varies to maintain one chip per 572mm² field at Introduction and two chips per 572mm² field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Cell area factor [a]	8	8	6	6	6	6	6
Cell area [$Ca = af^2$] (μm^2)	0.130	0.103	0.061	0.049	0.039	0.031	0.024
Cell array area at introduction (% of chip size) §	71.3%	71.8%	72.2%	72.6%	72.9%	73.2%	73.5%
Generation at introduction §	2G	2G	4G	4G	8G	8G	16G
Functions per chip (Gbits)	2.15	2.15	4.29	4.29	8.59	8.59	17.18
Chip size at introduction (mm^2) §	390	308	364	287	454	359	568
Gbits/cm^2 at introduction §	0.55	0.70	1.18	1.49	1.89	2.39	3.03

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Cell area factor [a]	6	4	4
Cell area [$Ca = af^2$] (μm^2)	0.012	0.004	0.002
Cell array area at introduction (% of chip size) §	74.2%	74.6%	74.9%
Generation at introduction §	32G	64G	64G
Functions per chip (Gbits)	34.36	68.72	68.72
Chip size at introduction (mm^2) §	563	373	186
Gbits/cm^2 at introduction §	6.10	18.42	37.00

Notes for Tables 1e and 1f:

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows:

1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

3. *at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and*
4. *at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).*

InTER-generation chip size growth rate varies to maintain one chip per 572mm² field at Introduction and two chips per 572mm² field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
SRAM Cell (6-transistor) Area factor ++	**126.1**	**123.0**	**120.3**	**117.8**	**115.6**	**113.7**	**111.9**
Logic Gate (4-transistor) Area factor ++	**320.0**	**320.0**	**320.0**	**320.0**	**320.0**	**320.0**	**320.0**
SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**
Logic Gate (4-transistor) Area efficiency ++	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**
SRAM Cell (6-transistor) Area w/overhead ++	**3.3**	**2.5**	**2.0**	**1.5**	**1.2**	**0.93**	**0.73**
Logic Gate (4-transistor) Area w/overhead ++	**10.4**	**8.2**	**6.5**	**5.2**	**4.1**	**3.3**	**2.6**
Transistor density SRAM (Mtransistors/cm^2)	**184**	**237**	**305**	**393**	**504**	**646**	**827**
Transistor density logic (Mtransistors/cm^2)	**38.6**	**48.6**	**61.2**	**77.2**	**97.2**	**122.5**	**154.3**
*Generation at introduction **	**p04c**	**—**	**—**	**p07c**	**—**	**—**	**p10c**
Functions per chip at introduction (million transistors [Mtransistors])	**193**	**243**	**307**	**386**	**487**	**614**	**773**
Chip size at introduction (mm^2) ‡	**280**	**280**	**280**	**280**	**280**	**280**	**280**
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**69**	**87**	**110**	**138**	**174**	**219**	**276**
*Generation at production **	**p01c**	**—**	**—**	**p04c**	**—**	**—**	**p07c**
Functions per chip at production (million transistors [Mtransistors])	**97**	**122**	**153**	**193**	**243**	**307**	**386**
Chip size at production (mm^2) §§	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**69.0**	**87.0**	**109.6**	**138.0**	**173.9**	**219.1**	**276.1**

Notes for Tables 1g and 1h:

++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples— the cost-performance processor, p01c, was introduced in 1999, but not ramped into volume production until 2001; similarly, the p04c, is introduced in 2001, but is targeted for volume production in 2004.*

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/1999), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5× every two-year technology node through 2001, then 0.5× every three-year technology node after 2001.

Refer to the Glossary for definitions

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years

YEAR OF PRODUCTION	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
SRAM Cell (6-transistor) Area factor ++	**107.8**	**106.7**	**105.7**
Logic Gate (4-transistor) Area factor ++	**320.0**	**320.0**	**320.0**
SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**
Logic Gate (4-transistor) Area efficiency ++	**0.50**	**0.50**	**0.50**
SRAM Cell (6-transistor) Area w/overhead ++	**0.22**	**0.17**	**0.13**
Logic Gate (4-transistor) Area w/overhead ++	**0.82**	**0.65**	**0.51**
Transistor density SRAM (Mtransistors/cm^2)	**1718**	**3532**	**7208**
Transistor density logic (Mtransistors/cm^2)	**309**	**617**	**1235**
*Generation at introduction **	**p13c**	**p16c**	**p19c**
Functions per chip at introduction (million transistors [Mtransistors])	**1546**	**3092**	**6184**
Chip size at introduction (mm^2) ‡	**280**	**280**	**280**
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**552**	**1104**	**2209**
*Generation at production **	**p10c**	**p13c**	**p16c**
Functions per chip at production (million transistors [Mtransistors])	**773**	**1546**	**3092**
Chip size at production (mm^2) §§	**140**	**140**	**140**
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**552**	**1104**	**2209**

Refer to the Glossary for definitions

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Logic (Low-volume Microprocessor) High-performance ‡							
*Generation at production ***	**p01h**	**—**	**p03h**	**—**	**p05h**	**—**	**p07h**
Functions per chip (million transistors)	**276**	**348**	**439**	**553**	**697**	**878**	**1106**
Chip size at production (mm^2) §§	**310**	**310**	**310**	**310**	**310**	**310**	**310**
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	**89**	**112**	**142**	**178**	**225**	**283**	**357**
ASIC							
ASIC usable Mtransistors/cm^2 (auto layout)	**89**	**112**	**142**	**178**	**225**	**283**	**357**
ASIC max chip size at production (mm^2) (maximum lithographic field size)	**800**	**800**	**572**	**572**	**572**	**572**	**572**
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**714**	**899**	**810**	**1020**	**1286**	**1620**	**2041**

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Logic (Low-volume Microprocessor) High-performance ‡			
*Generation at production ***	**—**	**p13h**	**—**
Functions per chip (million transistors)	**2212**	**4424**	**8848**
Chip size at production (mm^2) §§	**310**	**310**	**310**
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	**714**	**1427**	**2854**
ASIC			
ASIC usable Mtransistors/cm^2 (auto layout)	**714**	**1427**	**2854**
ASIC maximum chip size at production (mm^2)(maximum lithographic field size)	**572**	**572**	**572**
ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	**4081**	**8163**	**16326**

Notes for Tables 1i and 1j:

*** p is processor, numerals reflect year of production; h indicates high-performance product. Examples—the high-performance processor, p99h, was ramped into volume production in 1999; similarly, the p01h, is introduced in 2001.*

‡ MPU High-performance Model—High-performance MPU includes large L2 and L3 on-chip SRAM (2MByte/1999) plus a larger logic core (P99h core = 25M transistor (Mtransistors) both SRAM and Logic functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5x every two-year technology node through 2001, then 0.5x every three-year technology node after 2001.

Refer to the Glossary for definitions

Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

(Note: 2001 Lithographic field sizes represent current capability)

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length(nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Lithography Field Size							
Lithography Field Size—area (mm^2)	**800**	**800**	**800**	**800**	**800**	**800**	**572**
Lithographic field size — length (mm)	**32**	**32**	**32**	**32**	**32**	**32**	**26**
Lithographic field size — width (mm)	**25**	**25**	**25**	**25**	**25**	**25**	**22**
Maximum Substrate Diameter (mm) — High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	**300**	**300**	**300**	**300**	**300**	**300**	**300**

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years

Year of Production	2010	2013	2016
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Lithography Field Size			
Maximum lithographic field size—area (mm^2)			
Lithography Field Size—area (mm^2)	**572**	**572**	**572**
Maximum lithographic field size—length (mm)	**26**	**26**	**26**
Maximum lithographic field size—width (mm)	**22**	**22**	**22**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)			
Bulk or epitaxial or SOI wafer	**300**	**450**	**450**

Refer to the Glossary for definitions

Table 3a   Performance of Packaged Chips: Number of Pads and Pins—Near-term Years

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Number of Chip I/Os (Number of Total Chip Pads) — Maximum							
Total pads—MPU	**3072**	**3072**	**3072**	**3072**	**3072**	**3072**	**3072**
Signal I/O—MPU (1/3 of total pads)	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**
Power and ground pads—MPU (2/3 of total pads)	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**
Total pads—ASIC high-performance	**3000**	**3200**	**3400**	**3600**	**4000**	**4200**	**4400**
Signal I/O pads—ASIC high-performance	**1500**	**1600**	**1700**	**1800**	**2000**	**2100**	**2200**
Power and ground pads—ASIC high-performance (½ of total pads)	**1500**	**1600**	**1700**	**1800**	**2000**	**2100**	**2200**
Number of Total Package Pins—Maximum [1]							
Microprocessor/controller, cost-performance	**480–1,200**	**480–1320**	**500–1452**	**500–1600**	**550–1760**	**550–1936**	**600–2140**
Microprocessor/controller, high-performance	**1200**	**1320**	**1452**	**1,600**	**1,760**	**1,936**	**2,140**
ASIC (high-performance)	**1700**	**1870**	**2057**	**2263**	**2489**	**2738**	**3012**

Notes for Tables 3a and 3b:

[1]   Pin counts will be limited for some applications where fine pitch array interconnect is used by PWB technology and system cost.

The highest pin count applications will as a result use larger pitches and larger package sizes.

The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2:1 to 1:4

Refer to the Glossary for definitions

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Number of Chip I/Os (Number of Total Chip Pads) — Maximum			
Total pads—MPU	**3840**	**4224**	**4416**
Signal I/O—MPU (1/3 of total pads)	**1280**	**1408**	**1472**
Power and ground pads—MPU (2/3 of total pads)	**2560**	**2816**	**2944**
Total pads—ASIC high-performance	**4800**	**5400**	**6000**
Signal I/O pads—ASIC high-performance	**2400**	**2700**	**3000**
Power and ground pads—ASIC high-performance (½ of total pads)	**2400**	**2700**	**3000**
Number of Total Package Pins—Maximum [1]			
Microprocessor/controller, cost-performance	**780–2782**	**1014–3616**	**1318–4702**
Microprocessor/controller, high-performance	**2782**	**3616**	**4702**
ASIC (high-performance)	**4009**	**5335**	**7100**

Refer to the Glossary for definitions

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Chip Pad Pitch (micron)							
Pad pitch—ball bond	**45**	**35**	**30**	**25**	**20**	**20**	**20**
Pad pitch—wedge bond	**40**	**35**	**30**	**25**	**20**	**20**	**20**
Pad Pitch—area array flip-chip (cost-performance, high-performance)	**160**	**160**	**150**	**150**	**130**	**130**	**120**
Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	**150**	**130**	**120**	**110**	**100**	**90**	**80**
Cost-Per-Pin							
Package cost (cents/pin) (cost-performance)—minimum–maximum	**0.80–1.60**	**0.75–1.44**	**0.70–1.30**	**0.66–1.17**	**0.61–1.06**	**0.56–1.03**	**0.64–1.00**
Package cost (cents/pin) (Memory)—minimum–maximum	**0.36–1.54**	**0.34–1.39**	**0.32–1.26**	**0.30–1.14**	**0.28–1.03**	**0.27–0.93**	**0.27–0.84**

Table 4b Performance and Package Chips: Pads, Cost—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Chip Pad Pitch (micron)			
Pad pitch—ball bond	**20**	**20**	**20**
Pad Pitch—wedge bond	**20**	**20**	**20**
Pad Pitch—area array (cost-performance, high-performance)	**90**	**80**	**70**
Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	**60**	**45**	**30**
Cost-Per-Pin			
Package cost (cents/pin) (cost-performance)— minimum–maximum	**0.49–0.98**	**0.42–0.93**	**0.36–0.79**
Package cost (cents/pin) (Memory)— minimum–maximum	**0.22–0.54**	**0.19–0.39**	**0.19–0.33**

Refer to the Glossary for definitions

Table 4c Performance and Package Chips: Frequency On-Chip Wiring Levels—Near-term Years

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Chip Frequency (MHz)							
On-chip local clock	**1,684**	**2,317**	**3,088**	**3,990**	**5,173**	**5,631**	**6,739**
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	**1,684**	**2,317**	**3,088**	**3,990**	**5,173**	**5,631**	**6,739**
Maximum number wiring levels—maximum	**7**	**8**	**8**	**8**	**9**	**9**	**9**
Maximum number wiring levels—minimum	**7**	**7**	**8**	**8**	**8**	**9**	**9**

Table 4d Performance and Package Chips: Frequency, On-Chip Wiring Levels—Long-term Years

YEAR OF PRODUCTION	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Chip Frequency (MHz)			
On-chip local clock	**11,511**	**19,348**	**28,751**
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	**11,511**	**19,348**	**28,751**
Maximum number wiring levels—maximum	**10**	**10**	**10**
Maximum number wiring levels—minimum	**9**	**9**	**10**

Note for Tables 4c and 4d:

[1] The off chip frequency is expected to increase for a small number of high speed pins which will be used in combination with a large number of lower speed pins

[2] In 2001, high-speed serial communications transceiver devices are achieving chip-board frequencies of 3.125 GHz using CMOS, and 10 GHz using SiGe. In 2002 it is expected that 10 GHz transceivers will be fabricated using CMOS. 40 GHz SiGe devices are expected in 2003. The roadmap for higher levels of integration with wider bus widths, is shown in the High Frequency Serial Communications section in the Test chapter.

Refer to the Glossary for definitions

Table 5a Electrical Defects—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	**1,963**	**2,493**	**2,148**	**2,748**	**1,752**	**2236**	**1426**
MPU Random Defect D_0 at production chip size and 83% yield (faults/m^2) §§	**1,356**	**1,356**	**1,356**	**1,356**	**1,356**	**1,356**	**1,356**
# Mask Levels – MPU	**25**	**25**	**25**	**25**	**25**	**27**	**27**
# Mask Levels – DRAM	**21**	**22**	**24**	**24**	**24**	**24**	**24**

Table 5b Electrical Defects—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	**1356**	**1356**	**1356**
MPU Random Defect D_0 at production chip size and 83% yield (faults/m^2) §§	**1464**	**1116**	**1134**
# Mask Levels – MPU	**27**	**29**	**29**
# Mask Levels – DRAM	**26**	**26**	**26**

Notes for Tables 5a and 5b:

D_0 — defect density

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows:

1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

1. *at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and*
2. *at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).*

InTER-generation chip size growth rate varies to maintain one chip per 572mm² field at Introduction and two chips per 572mm² field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5× every two-year technology node through 2001, then 0.5× every three-year technology node after 2001.

Refer to the Glossary for definitions

Table 6a Power Supply and Power Dissipation—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Power Supply Voltage (V)							
V_{dd} *(high performance)*	**1.1**	**1.0**	**1.0**	**1**	**0.9**	**0.9**	**0.7**
V_{dd} *(Low Operating Power, high* V_{dd} *transistors)*	**1.2**	**1.2**	**1.1**	**1.1**	**1.0**	**1.0**	**0.9**
V_{dd} *(Low Standby Power, high* V_{dd} *transistors)*	**1.2**	**1.2**	**1.2**	**1.2**	**1.2**	**1.2**	**1.1**
Allowable Maximum Power [1]							
High-performance with heatsink (W)	**130**	**140**	**150**	**160**	**170**	**180**	**190**
Cost-performance (W)	**61**	**75**	**81**	**85**	**92**	**98**	**104**
Battery (W)—(hand-held)	**2.4**	**2.6**	**2.8**	**3.2**	**3.2**	**3.5**	**3.5**

Table 6b Power Supply and Power Dissipation—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Power Supply Voltage (V)			
V_{dd} *(high performance)*	**0.6**	**0.5**	**0.4**
V_{dd} *(Low Operating Power, high* V_{dd} *transistors)*	**0.8**	**0.7**	**0.6**
V_{dd} *(Low Standby Power, high* V_{dd} *transistors)*	**1.0**	**0.9**	**0.9**
Allowable Maximum Power [1]			
High-performance with heatsink (W)	**218**	**251**	**288**
Cost-performance (W)	**120**	**138**	**158**
Battery (W)—(hand-held)	**3.0**	**3.0**	**3.0**

Note for Table 6a and 6b:

[1]   Power will be limited more by system level cooling and test constraints than packaging

Refer to the Glossary for definitions

Table 7a Cost—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	**21**	**14.8**	**10.5**	**7.4**	**5.3**	**3.7**	**2.6**
DRAM cost/bit at (packaged microcents) at production §	**7.7**	**5.4**	**3.8**	**2.7**	**1.9**	**1.4**	**0.96**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**176**	**124**	**88**	**62**	**44**	**31**	**22**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**107**	**75**	**53**	**38**	**27**	**19**	**13.3**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**97**	**69**	**49**	**34**	**24**	**17**	**12**
Cost-Per-Pin							
Test Cost							
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	**4.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**

Notes for Tables 7a and 7b:

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two-four years after introduction).

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows:
1999–2002/8×; 2003–2010/6×; 2011–2016/4×.
DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

1. *at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and*
2. *at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).*

InTER-generation chip size growth rate varies to maintain one chip per 572mm² field at Introduction and two chips per 572mm² field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5× every two-year technology node through 2001, then 0.5× every three-year technology node after 2001.

Refer to the Glossary for definitions

Table 7b Cost—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Affordable Cost per Function ++			
DRAM cost/bit (packaged microcents) at samples/introduction	0.93	0.33	0.12
DRAM cost/bit (packaged microcents) at production §	0.34	0.12	0.042
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78	2.75	0.97
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71	1.66	0.59
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.31	1.52	0.54
Cost-Per-Pin			
Test Cost			
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	4	4	4
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	2	3	4

Refer to the Glossary for definitions

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

Technology Node—The ground rules of process governed by the smallest feature printed. The half-pitch of first-level interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. For logic, such as microprocessors (MPUs), physical bottom gate length is most representative of the leading-edge technology level required for maximum performance. MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first polysilicon or metal layer and lags behind DRAM half-pitch, which may also refer either first layer metal or polysilicon. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology node step represents the creation of significant technology progress—approximately 70% of the preceding node, 50% of two preceding nodes. Example: DRAM half pitches of 180, 130, 90, 65, 45, 32 nm, and 22 nm. For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

Moore's Law—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore's Law, there is a historically-based "corollary" to the "law," which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every two years, as suggested by consensus DRAM and MPU models of the *1999 ITRS*, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1Mbytes/2001). Logic functionality and L2 cache typically double every two-year generation.

High-performance MPU—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example 2@ 25Mt cores in 2001) with a large (example 4Mbyte/2001) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two-year generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology-node scaling (.7× linear, .5× area) is every three years, an additional device/process design improvement of .8× per two years must be achieved. This requirement represents a design-related (cell-area-factor) area-reduction improvement of at least -11% per year, , and this design-related productivity improvement is in addition to the basic lithography-based area reduction of -21% per year (three-year node cycle). The present *2001 ITRS* consensus target for the rate of increase of DRAM is 2×/chip every two years. However, the *2001 ITRS* forecast of cell-area-factor improvement is only -7% per year on average. This results in an average DRAM inTER-generation chip-size growth of 4.5%/year or about 1.2× every four years. Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the *2001 ITRS* MPU inTER-generation functionality model target is 2× transistors/chip every technology node, in order maintain a flat chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The *2001 ITRS* consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The *ITRS* targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three years at the leading-edge process technology node, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples.
Example: 1997/ISSCC/1Gb DRAM, versus *ITRS* 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every two years (every technology node, in the case of MPUs). In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat, or at the most, 1.2× every four years.

Year Of PRODUCTION—Year in which leading chip manufacturers begin shipping volume quantities (10K/month) of product manufactured with qualified production tooling and processes and is followed within three months by a second manufacturer. As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity. For high-demand products, volume production typically continues to ramp to fab design capacity within 12 months. Alpha-level manufacturing tools and research technology papers are typically delivered 24 months prior to volume production ramp. Beta-level tools are typically delivered 12 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1Gb/production, 4G/introduction, plus 512Mb/256Mb/128Mb/64Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the *ITRS* consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the *2001 ITRS*, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 55% at the production level, and less than 50% at the ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified *ITRS*-consensus Cell Area Factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated , which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$. The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE} . Example: 1999: A=8; square of the half-pitch, $f^2= (180\ nm)^2=.032\ \mu m^2$; cell area, $C=Af^2=0.26\ \mu m^2$; for 1Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E=0.37\ \mu m^2$; therefore, the 1Gb Chip Size Area=2^{30} bits * 0.37e-6 mm^2/bit = 397 mm^2.

DRAM Cell Area Factor—A number (A) which expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, 1.6×1.6=2.5, etc.).

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-Performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-Performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The *ITRS* timing targets, contributed by the Factory Integration ITWG, are based on the first 20K wafer-starts-per-month manufacturing facility.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins. **BACK TO TOP**