



ITRS Conference 2002

July 24, 2002 San Francisco, California

ITRS 2002 Yield Enhancement Update

Milton Godwin
Applied Materials

2001 ITRS YE ITWG Co-chairs

- **United States**
 - Christopher Long
 - IBM
 - Milt Godwin
 - Applied Materials MDR
- **Taiwan**
 - TBD
- **Korea**
 - TBD
- **Europe**
 - Lothar Pfitzner
 - Fraunhofer Institute
- **Japan**
 - Toshihiko Osada
 - Fujitsu
 - Hiroshi Kitajima
 - NEC



International Technology Roadmap for Semiconductors

24 July 2002 Work In Progress – Not for Publication

ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- Attendees:
 - Lothar Pfitzner Fraunhofer Institute
 - Andreas Nutsch Fraunhofer Institute
 - Ines Thurner Infineon Technologies
 - Manuela Huber Infineon Technologies
 - Dick Verkleij FEI/Philips Semiconductors
 - Toshihiko Osada Fujitsu
 - Milt Godwin Applied Materials
- Gracious thanks to Lothar and Andreas who hosted and supported our visit to Fraunhofer Institute.



2001 ITRS Yield Enhancement US Domestic TWG Membership

- **Yield Model and Defect Budget**
 - Honey Goel - Chair (TI)
 - Darren Dance (WWK)
 - Dan Maynard (IBM)
 - Mel Efron (HPL)
 - Manuela Huber (Infineon)
- **Defect Detection and Characterization**
 - Mike Retersdorf – Chair (AMD)
 - Bob Bryant (n-Line)
 - Walt Gardner (ORNL)
 - Paul Jones (n-Line)
 - Matthew Sbragia (TSK)
 - Rick Jarvis – Chair (AMD)
- **Yield Learning**
 - Fred Lakhani – Chair (ISMT)
 - Hank Walker (Texas A+M)
 - Ken Tobin (ORNL)
 - Dave Chamness (Agilent)
 - Mike McIntyre (AMD)
- **Wafer Environment Contamination Control**
 - Chris Long – Chair (IBM)
 - Bill Fil (IBM)
 - Ralph Richardson (Air Products)
 - Dianne Dougherty (ChemTrace)
 - James McAndrew (AirLiquide)
 - Michael Patterson (Intel)
 - Jeff Chapman (IBM)



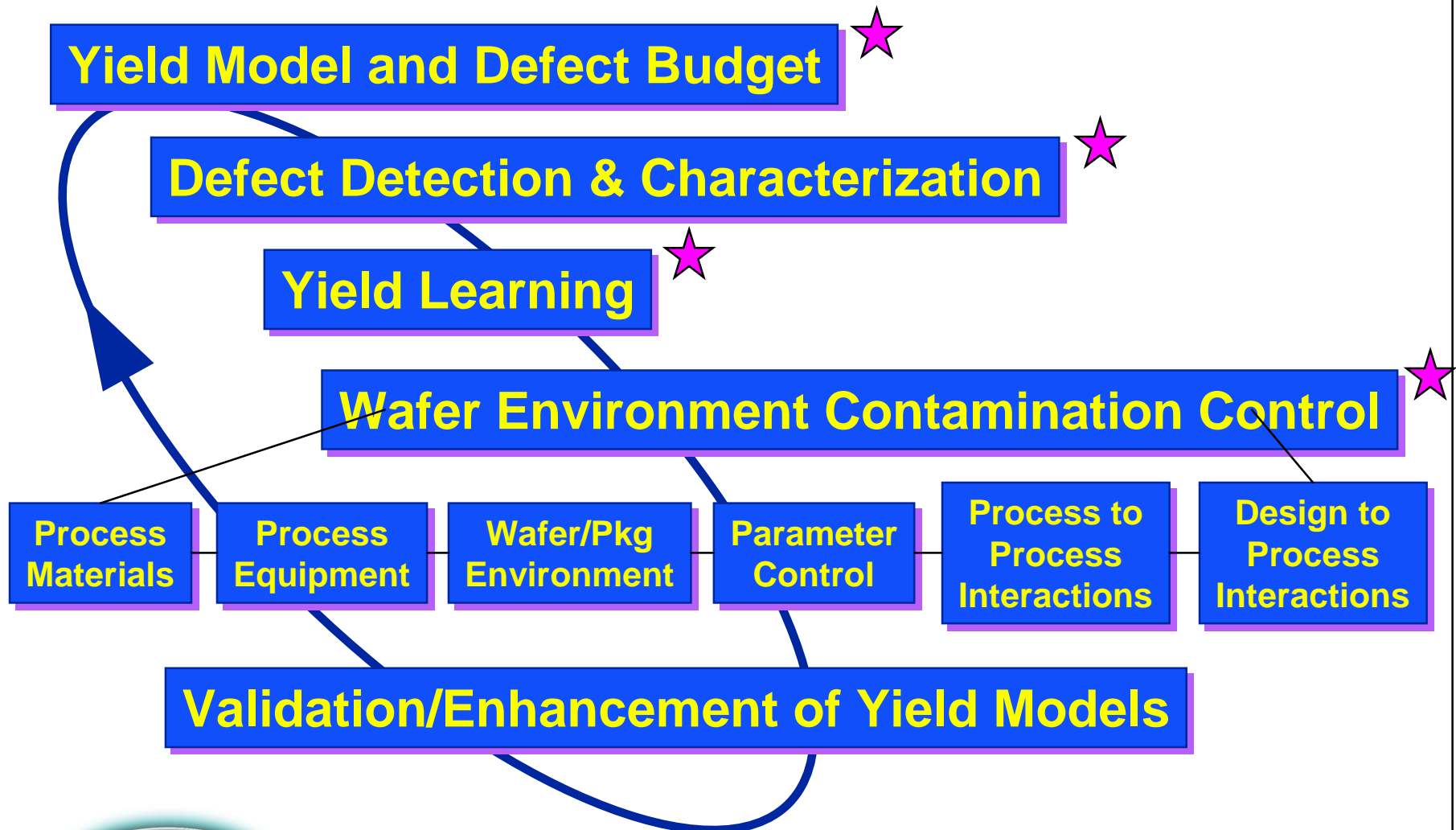
2001 ITRS Defect Reduction JEITA WG11 Membership

Toshihiko Osada (C)	Fujitsu
Hiroshi Kitajima(C)	NEC
Fumio Mizuno	Neisei Univ.
Masahiko Ikeno	Mitsubishi
Ichiro Nakao	National/Panasonic
Motosuke Miyoshi	Toshiba
Makoto Akizuki	Sanyo
Masanori Takahashi	Seiko
Norio Moriyama	Oki
Hideyuki Sakaizawa	TSK
Masakazu Ichikawa	JRCAT



Yield Enhancement TWG Yield Learning Cycle

★ Focus Topics



International Technology Roadmap for Semiconductors

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YE Difficult Challenges

>65nm, Approaching 2007

- **Yield Models**

- Random, systematic, parametric, and memory redundancy models must be developed and validated to correlate process-induced defects (PID), particle counts per wafer pass (PWP), and *in situ* tool/process measurements to yield.

- **High-Aspect-Ratio Inspection.**

- High-speed, cost-effective tools must be developed that rapidly detect defects at approximately 1/3 X ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches and especially defects near or at the bottoms of these features.
- *Defect/Fault Sourcing for Rapid Yield Learning.*
- Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test, and work-in-process (WIP) data must be developed to enable the rapid root-cause analysis of yield-limiting conditions.



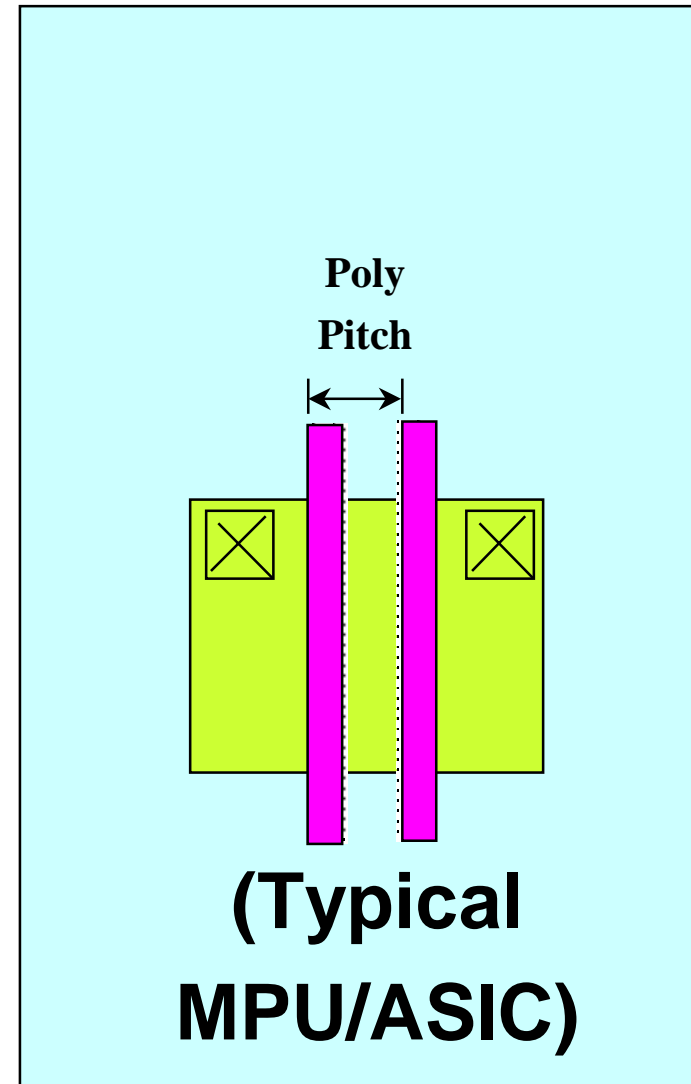
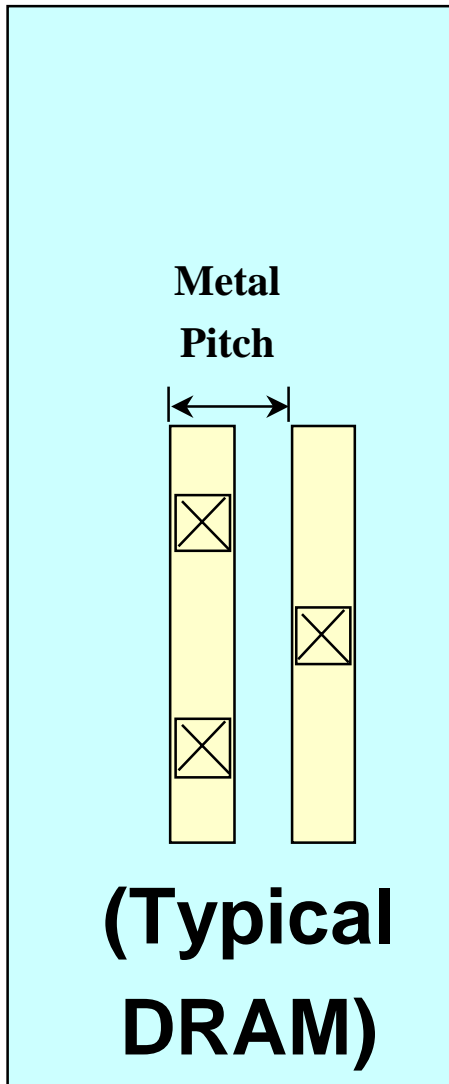
YE Difficult Challenges (cont.)

>65nm, Approaching 2007

- **Correlation of Impurity Level to Yield.**
 - Methodology for employment and correlation of fluid/gas contamination types to yield of a standard test structure or product.
- **Non-visual Defect Sourcing**
 - Failure analysis tools and techniques are required to enable localization of defects where no visual defect is detected.
- **Design for Manufacture and Test**
 - IC designs must be optimized for a given process capability and must be testable and diagnosable.



Technology Node -Half Pitch (= Pitch/2) Definition



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- Changes in Tables for 2002 Update
 - **Tables 89, 90, and 91:**
 - **Cluster parameters used in the calculation of Tables 90 and 91 should be designated as 2, not 5.**



Yield Model and Defect Budget

MPU - Technology Requirements:

Table 90 Yield Model and Defect Budget MPU Technology Requirements

Year of Introduction "Technology Node"	2001 130nm	2002 115 nm	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
MPU										
MPU 1/2 metal 1 pitch (nm) (A)	150	130	107	90	80	70	65	45	32	22
Critical Defect Size (nm)	75	65	54	45	40	35	33	23	16	11
Chip Size (mm ²) (B)	140	140	140	140	140	140	140	140	140	140
Overall Electrical D ₀ (faults/m ²) at critical defect size or greater (C)	2115	2115	2115	2115	2115	2115	2115	2115	2115	2115
Random D ₀ (faults/m ²) (D)	1356	1356	1356	1356	1356	1356	1356	1356	1356	1356
# Mask Levels (E)	25	25	25	25	25	27	27	27	29	29
Random Faults/Mask	54	54	54	54	54	50	50	50	47	47

- **Key Assumptions:**
 - Volume production
 - Based on cost performance MPU
 - Overall Sort Yield (Y_{sort} = 75%)
 - Systematic Limited Yield (Y_s ~ 90%)
 - Random Defect Limited Yield (Y_r ~ 83%)



Yield Model and Defect Budget

MPU - Technology Requirements:

Year of Introduction "Technology Node"	2001 130nm	2002 115 nm	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
MPU Random Particles per Wafer pass (PWP) Budget (defects/m²) for Generic Tool Type scaled to 75nm critical defect size or greater (F)										
CMP Clean	448	337	228	161	127	90	78	37	18	8
CMP Insulator	1084	814	552	390	308	219	189	90	43	20
CMP Metal	1225	920	623	441	348	247	213	102	48	23
Coat/Develop/Bake	196	147	100	70	56	39	34	16	8	4
CVD Insulator	963	772	523	370	292	207	179	86	40	19
CVD Oxide Mask	1267	950	644	455	360	255	220	105	50	23
Dielectric Track	308	232	157	111	88	62	54	26	12	6
Furnace CVD	549	412	279	198	156	111	95	46	22	10
Furnace Fast Ramp	497	373	253	179	141	100	86	41	19	9
Furnace Oxide/Anneal	321	241	164	116	91	65	56	27	13	6
Implant High Current	430	323	219	155	122	87	75	36	17	8
Implant Low/Med Current	392	295	200	141	112	79	68	33	15	7
Inspect PLY	400	300	203	144	114	81	70	33	16	7
Inspect Visual	429	323	219	155	122	87	75	36	17	8
Litho Cell	332	250	169	120	95	67	58	28	13	6
Litho Stepper	315	237	160	113	90	64	55	26	12	6
Measure CD	374	281	190	135	106	75	65	31	15	7
Measure Film	321	241	164	116	91	65	56	27	13	6
Measure Overlay	298	224	152	107	85	60	52	25	12	6
Metal CVD	585	439	298	211	166	118	102	49	23	11
Metal Electroplate	302	227	154	109	86	61	52	25	12	6
Metal Etch	1300	976	661	468	370	262	226	108	51	24
Metal PVD	667	501	339	240	190	135	116	56	26	12
Plasma Etch	1183	889	602	426	336	239	206	99	46	22
Plasma Strip	547	411	278	197	156	110	95	46	21	10
RTP CVD	357	268	181	128	101	72	62	30	14	7
RTP Oxide/Anneal	234	175	119	84	66	47	41	19	9	4
Test	91	69	47	33	26	18	16	8	4	2
Vapor Phase Clean	822	617	418	296	234	166	143	68	32	15
Wafer Handling	37	28	19	13	10	7	6	3	1	1
Wet Bench	535	402	272	192	152	108	93	45	21	10



Yield Model and Defect Budget

DRAM - Technology Requirements:

Table 91 Yield Model and Defect Budget DRAM Technology Requirements

Year of Introduction "Technology Node"	2001 130nm	2002 115 nm	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
DRAM										
DRAM 1/2 metal 1 pitch (nm) (A)	130	115	100	90	80	70	65	45	32	22
Critical Defect Size (nm)	65	58	50	45	40	35	33	23	16	11
Chip Size (mm ²) (B)	127	100	118	93	147	116	183	181	240	238
Cell Array Area (%) @ Production	55%	55%	56%	56%	56%	57%	57%	58%	58%	58%
Non-Core Area (mm ²)	57	45	52	41	64	50	79	77	101	99
Overall Electrical D ₀ (faults/m ²) at critical defect size or greater (C)	2890	3671	3163	4047	2580	3293	2100	2155	1643	1670
Random D ₀ (faults/m ²) (D)	1963	2493	2148	2748	1752	2236	1426	1464	1116	1134
# Mask Levels (E)	21	22	24	24	24	24	24	26	26	26
Random Faults/Mask	93	113	89	115	73	93	59	56	43	44

• Key Assumptions:

- Volume production
- Overall Sort Yield ($Y_{\text{sort}} = Y_s * Y_r = 85\%$)
- Systematic Limited Yield ($Y_s \sim 95\%$)
- Random Defect Limited Yield ($Y_r \sim 89.5\%$)
- Core area of DRAM enough redundancy to obtain overall yield target



Yield Model and Defect Budget

DRAM - Technology Requirements:

Year of Introduction "Technology Node"	2001 130nm	2002 115 nm	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
DRAM Random Paritcle per Wafer pass (PWP) Budget (defects/m2) for Generic Tool Type scaled to 75nm critical defect size or greater (F)										
CMP Clean	1076	1021	610	632	318	311	171	78	30	14
CMP Insulator	833	790	472	489	246	241	132	60	23	11
CMP Metal	1276	1211	723	750	378	369	203	92	36	17
Coat/Develop/Bake	333	316	188	195	98	96	53	24	9	4
CVD Insulator	923	876	523	542	273	267	147	67	26	12
CVD Oxide Mask	1133	1075	642	665	335	327	180	82	32	15
Dielectric Track	467	443	264	274	138	135	74	34	13	6
Furnace CVD	638	605	361	374	189	184	101	46	18	9
Furnace Fast Ramp	601	571	341	353	178	174	96	43	17	8
Furnace Oxide/Anneal	481	456	272	282	142	139	76	35	13	6
Implant High Current	559	530	316	328	165	161	89	40	16	7
Implant Low/Med Current	533	506	302	313	158	154	85	38	15	7
Inspect PLY	729	691	413	428	216	211	116	53	20	10
Inspect Visual	752	713	426	441	222	217	119	54	21	10
Litho Cell	624	592	354	367	185	180	99	45	17	8
Litho Stepper	415	394	235	244	123	120	66	30	12	6
Measure CD	623	591	353	366	184	180	99	45	17	8
Measure Film	586	556	332	344	173	169	93	42	16	8
Measure Overlay	570	541	323	335	169	165	91	41	16	8
Metal CVD	587	557	333	345	174	170	93	42	16	8
Metal Electroplate	446	423	253	262	132	129	71	32	12	6
Metal Etch	1080	1025	612	634	320	312	172	78	30	14
Metal PVD	644	611	365	378	191	186	102	46	18	9
Plasma Etch	1144	1085	648	672	338	331	182	83	32	15
Plasma Strip	878	833	497	516	260	254	140	63	24	12
RTP CVD	574	545	325	337	170	166	91	41	16	8
RTP Oxide/Anneal	420	398	238	247	124	121	67	30	12	6
Test	82	78	46	48	24	24	13	6	2	1
Vapor Phase Clean	1215	1152	688	713	359	351	193	88	34	16
Wafer Handling	34	33	20	20	10	10	5	2	1	0
Wet Bench	870	825	493	511	257	251	138	63	24	12



Yield Model and Defect Budget

Key messages

- **Yield targets will be tough to reach in future**
 - **Requires work in different areas:**
 - Tool defect budget:
 - > reduced defectivity for equipment (ITRS gives guidance for targets)
 - Process induced defect budget
 - > better understanding of new integration issues, materials, etc.
 - Systematic limited yield area (main focus in future)
 - > Design for manufacturability
 - > Process control, Equipment control, new materials issues, etc.
- > Future: more emphasis on Yield Ramp needed**



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- Changes in Tables for 2002 Update
 - **Table 93a:**
 - **Unpatterned PSL spheres: Lines designated as 0.5x DR but are not.**
 - **Footnote D for Unpatterned Wafers must include requirements of haze maximally suppressed and minimal COP detection.**
 - **Yield Ramp at 1200 cm²/hr: @005 entry should be 64, not 65**
 - **Wafer backside 200mm (# events flip method): 2005 and 2006 entries should be 1000, not 2000.**
 - **Unpatterned PSL spheres: Metal Film line should be 62 in 2004, not 32?**



Table 93: Defect Detection Technology Requirements - Short Term

Table 93a Defect Detection Technology Requirements—Near-term

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007	DRIVER
	130 nm	115nm	100nm	90 nm	80nm	70nm	65nm	
<i>Patterned Wafer Inspection, PSL* Spheres at 90% Capture, Equivalent Sensitivity (nm) [A, B]</i>								
Process R&D at 300 cm ² /hr (1 wafer/hr)	78	72	66	54	48	42	39	0.6 x DR
Yield ramp at 1200 cm ² /hr (4 wafer/hr)	104	96	88	72	65	56	52	0.8 x DR
Volume production at 3000 cm ² /hr (10 wafer/hr)	130	120	110	90	80	70	66	1.0 x DR
<i>High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[C]</i>								
All stages of manufacturing	130	120	110	90	80	70	65	1.0 x DR
Process verification (1 wafer/hr)	130	120	110	90	80	70	65	1.0 x DR
Volume manufacturing (4 wafer/hr)	130	120	110	90	80	70	65	1.0 x DR
Cost of Ownership :volume manufacturing, non-HARI (\$/wafer scanned, 10/hr)	2-5	2-5	2-5	3-7	3-7	3-7	3-7	
CoO HARI	20-50	20-50	20-50	20-50	20-50	20-50	20-50	
<i>Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[D, E, I]</i>								
Metal film	91	85	77	63	56	49	33	0.7 x DR
Nonmetal films	70	65	59	49	43	35	33	0.5 x DR
Bare silicon	70	65	59	49	43	35	33	0.5 x DR
Wafer backside 200mm (# events flip method)	2500	2000	2000	2000	2000	2000	1000	
Wafer backside 200mm (defect size nm)	200	200	200	200	100	100	100	
<i>Defect Review (Patterned wafer)</i>								
Resolution (nm) *[F]	7	7	6	5	5	4	3	0.05 x DR
Coordinate accuracy (µm) at resolution	2	2	1	1	1	1	1	(J)
Coordinate accuracy (µm) at size	15	12	12	10	10	7	7	
<i>Automatic Defect Classification at Defect Review Platform *[G, H]</i>								
Redetection: minimum defect size (nm)	52	48	44	36	30	28	26	0.4 x DR
Number of defect types	10	10	10	15	15	15	15	[K]
Speed (seconds/defect)	7	5	5	5	5	5	5	
Speed w/elemental (seconds/defect)	20	15	13	10	10	10	10	

*polystyrene latex ; spheres utilized to simulate defects of known size during sizing calibration.



Table 93: Defect Detection Technology Requirements - Short Term

Table 93a Defect Detection Technology Requirements—Near-term

#1

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007	DRIVER
	130 nm	115nm	100nm	90 nm	80nm	70nm	65nm	
<i>Patterned Wafer Inspection, PSL* Spheres at 90% Capture, Equivalent Sensitivity (nm) [A, B]</i>								
Process R&D at 300 cm ² /hr (1 wafer/hr)	78	72	66	54	48	42	39	0.6 x DR
Yield ramp at 1200 cm ² /hr (4 wafer/hr)	104	96	88	72	65	56	52	0.8 x DR
Volume production at 3000 cm ² /hr (10 wafer/hr)	130	120	110	90	80	70	66	1.0 x DR
<i>High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[C]</i>								
All stages of manufacturing	130	120	110	90	80	70	65	1.0 x DR
Process verification (1 wafer/hr)	130	120	110	90	80	70	65	1.0 x DR
Volume manufacturing (4 wafer/hr)	130	120	110	90	80	70	65	1.0 x DR
Cost of Ownership :volume manufacturing, non-HARI (\$/wafer scanned, 10/hr)	2-5	2-5	2-5	3-7	3-7	3-7	3-7	
CoO HARI	20-50	20-50	20-50	20-50	20-50	20-50	20-50	
<i>Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[D, E, I]</i>								
Metal film	91	85	77	63	56	49	33	0.7 x DR
Nonmetal films	70	65	59	49	43	35	33	0.5 x DR
Bare silicon	70	65	59	49	43	35	33	0.5 x DR
Wafer backside 200mm (# events flip method)	2500	2000	2000	2000	2000	2000	1000	
Wafer backside 200mm (defect size nm)	200	200	200	200	100	100	100	
<i>Defect Review (Patterned wafer)</i>								
Resolution (nm) *[F]	7	7	6	5	5	4	3	0.05 x DR
Coordinate accuracy (µm) at resolution	2	2	1	1	1	1	1	(J)
Coordinate accuracy (µm) at size	15	12	12	10	10	7	7	
<i>Automatic Defect Classification at Defect Review Platform *[G, H]</i>								
Redetection: minimum defect size (nm)	52	48	44	36	30	28	26	0.4 x DR
Number of defect types	10	10	10	15	15	15	15	[K]
Speed (seconds/defect)	7	5	5	5	5	5	5	
Speed w/elemental (seconds/defect)	20	15	13	10	10	10	10	

*polystyrene latex ; spheres utilized to simulate defects of known size during sizing calibration.



Defect Detection and Characterization

Key Issues for 2002 #1

- There is an error in the table 93 as currently available from the ISMT ITRS website
 - The unpatterned inspection row for Metal Films has a driver that should be about .7X (not the .5 indicated).
 - The boxes should be **Red** below the 60nm level. (Barrier metals is the driver due to number of deps per process flow.)
- The **Yellow** boxes indicate that previous processing defects and variations in films and silicon quality make maintenance of these recipes more frequent than desired.
- Recipe parameters are usually set very close to nominal process window variation, therefore causing numerous occasions for engineering intensive analysis.



Table 93: Defect Detection Technology Requirements - Short Term

Table 93a Defect Detection Technology Requirements—Near-term

#2

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007	DRIVER
	130 nm	115nm	100nm	90 nm	80nm	70nm	65nm	
<i>Patterned Wafer Inspection, PSL* Spheres at 90% Capture, Equivalent Sensitivity (nm) [A, B]</i>								
Process R&D at 300 cm ² /hr (1 wafer/hr)	78	72	66	54	48	42	39	0.6 x DR
Yield ramp at 1200 cm ² /hr (4 wafer/hr)	104	96	88	72	65	56	52	0.8 x DR
Volume production at 3000 cm ² /hr (10 wafer/hr)	130	120	110	90	80	70	66	1.0 x DR
<i>High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[C]</i>								
All stages of manufacturing	130	120	110	90	80	70	65	1.0 x DR
Process verification (1 wafer/hr)	130	120	110	90	80	70	65	1.0 x DR
Volume manufacturing (4 wafer/hr)	130	120	110	90	80	70	65	1.0 x DR
Cost of Ownership :volume manufacturing, non-HARI (\$/wafer scanned, 10/hr)	2-5	2-5	2-5	3-7	3-7	3-7	3-7	
CoO HARI	20-50	20-50	20-50	20-50	20-50	20-50	20-50	
<i>Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[D, E, I]</i>								
Metal film	91	85	77	63	56	49	33	0.7 x DR
Nonmetal films	70	65	59	49	43	35	33	0.5 x DR
Bare silicon	70	65	59	49	43	35	33	0.5 x DR
Wafer backside 200mm (# events flip method)	2500	2000	2000	2000	2000	2000	1000	
Wafer backside 200mm (defect size nm)	200	200	200	200	100	100	100	
<i>Defect Review (Patterned wafer)</i>								
Resolution (nm) *[F]	7	7	6	5	5	4	3	0.05 x DR
Coordinate accuracy (µm) at resolution	2	2	1	1	1	1	1	(J)
Coordinate accuracy (µm) at size	15	12	12	10	10	7	7	
<i>Automatic Defect Classification at Defect Review Platform *[G, H]</i>								
Redetection: minimum defect size (nm)	52	48	44	36	30	28	26	0.4 x DR
Number of defect types	10	10	10	15	15	15	15	[K]
Speed (seconds/defect)	7	5	5	5	5	5	5	
Speed w/elemental (seconds/defect)	20	15	13	10	10	10	10	

*polystyrene latex ; spheres utilized to simulate defects of known size during sizing calibration.



Defect Detection and Characterization

Key Issues for 2002

#2

- There is need to enhance the speed for ADC, especially SEM, below the 5 secs per defect for redetection, imaging, and ADC.
 - The accuracy of ADC drives the capital expense need, BUT
 - The speed needs to exceed human speed per classified defect
 - 5000 WS/week and defect levels from FEOL drive the number of ADC samples
 - One model is : 15 mins per lot with 4 wafers sampled, 80 defects/wfr
- EDX spectrums are the next required information/defect
 - This might be a subset of the ADC results, but dwell time per defect is not at expectation and increases Defect Review time to almost 2 hours per lot
 - Smart sampling is required if current dwell times are not improved.



Yield Learning Optimization

Key Elements of Optimal Yield Learning:

- Design to process compatibility
- Testability and diagnosability
- Technology development and transfer
- Available cycles of learning
- Detection, sourcing & elimination of defects/faults



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- Changes in Tables for 2002 Update (continued)
 - **Table 94:**
 - **Line: # of mask levels should follow latest IRC update; if DRAM, then designate; if MPU, then designate.**
 - **Line: # of processing steps; assuming number is for 3-metal DRAM; number is too low.**
 - **Line: Cycle Time; 25 is too short (foundry?), must be greater number (35-45 days?)**
 - **Line: Average number of inspection/lot; 7 in ramp w/o critical photo steps, 13 in production of 2-level metal**
 - **Footnote D: Should assume 10% sampling, then change DV row**
 - **Line: Time to Recognize Electrical Fault Signature; should be average cycle time**
 - **Line: Time to Identify Defect Mechanism – weeks to months**



Defect/Fault Sourcing Complexity

Budget Category	Year of First Product Shipment (Technology Generation)					
	2001 (130nm)	2004 (90nm)	2007 (65nm)	2010 (45nm)	2013 (32nm)	2016 (22nm)
Critical Defect Size	65nm	45nm	33nm	23nm	16nm	11nm
Logic Transistor Density/cm ² (1E6)	14	35	85	210	519	1279
No. of process steps	490	530	570	610	650	690
Defect/Fault Sourcing Complexity Factor (1E9)	7	18	49	128	337	883
Defect/Fault Sourcing Complexity Trend (normalized to 130nm node)	1	3	7	18	48	126



Table 94a: Yield Learning Technology Requirements - Near Term

Table 94a Yield Learning Technology Requirements—Near-term

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch	130nm	115nm	100nm	90nm	80nm	70nm	65nm
MPU Printed Gate Length	90nm	75nm	65nm	53nm	45nm	40nm	35nm
Wafer size (mm)	300	300	300	300	300	300	300
Number of mask levels	25	25	25	27	27	27	29
Number of processing steps	490	503	516	530	543	556	570
Cycle time during ramp (# days)	25	25	25	27	27	27	29
<i>Defect/Fault Sourcing Complexity [A], [G]</i>							
Logic transistor density/cm ² (1E6)	14	19	26	35	47	63	85
Defect sourcing complexity factor (1E9) [B]	7	10	13	18	25	35	49
Defect sourcing complexity trend [C]	1	1	2	3	4	5	7
<i>Data Analysis for Rapid Defect/Fault Sourcing</i>							
Pattern wafer inspection sensitivity (nm) during ramp	104	96	88	72	64	56	52
Average # of inspections/wafer during full flow	5	5	5	5.4	5.4	5.4	5.8
Defect data volume (# data items/wafer) (1E13) [D]	5.5	7.1	9.4	12.5	15.8	20.7	25.7
Defect data volume (DV) trend [E]	1	1	2	2	3	4	5
<i>Yield Learning During Ramp from 30% to 80% Sort Yield [F]</i>							
# Learning cycles/year based on full flow cycle time	14.6	14.6	14.6	13.5	13.5	13.5	12.6
Required yield improvement rate per learning cycle	3.4	3.4	3.4	3.7	3.7	3.7	4.0
Time to i.d./ fix new defect/fault source during ramp	12.5	12.5	12.5	13.5	13.5	13.5	14.5
# Learning cycles/yr for 1 defect/fault source/month	8.6	8.6	8.6	7.5	7.5	7.5	6.6
Req yield improvement rate/learning cycle for 1 defect/fault source/month	5.8	5.8	5.8	6.7	6.7	6.7	7.6



Table 94b: Yield Learning Technology Requirements - Long Term

Table 94b Yield Learning Technology Requirements—Long-term

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ PITCH	45nm	32nm	22nm
MPU PRINTED GATE LENGTH	25	18	13
Wafer size (mm)	450	450	450
Number of mask levels	31	33	35
Number of processing steps	610	650	690
Cycle time during ramp (# days)	31	33	35
<i>Defect/Fault Sourcing Complexity [A], [G]</i>			
Logic transistor density/cm ² (1E6)	210	519	1279
Defect sourcing complexity factor (1E9) [B]	128	337	883
Defect sourcing complexity trend [C]	18	48	126
<i>Data Analysis for Rapid Defect/Fault Sourcing</i>			
Patterned wafer inspection sensitivity (nm) during yield ramp	18	13	9
Average # of inspections/wafer during full flow	6.2	6.6	7
(# data items/wafer) (1E13) [D]	57.4	120.8	271.2
Defect data volume (DV) trend [E]	1u	22	49
<i>Yield Learning During Ramp from 30% to 80% sort yield [F]</i>			
# of yield learning cycles/year based on full flow cycle time	11.8	11.1	10.4
Required yield improvement rate per learning cycle	4.2	4.5	4.8
Time to identify and fix new defect/fault source during ramp	15.5	16.5	17.5
# of learning cycles/year for 1 defect/fault source/month	5.8	5.1	4.4
Required yield improvement rate/learning cycle for 1 defect/fault source/month	8.7	9.9	11.3



Yield Learning Challenges

- Data Analysis for Rapid Defect/Fault Sourcing: Increasing defect sourcing complexity and data volume will challenge both defect sourcing tools and data management tools to identify and source:
- **visible defects**
 - non-visual defects
 - electrical parametric issues
 - electrical faults at sort and final test
 - interactions between design, process and test
- Yield Learning During Ramp from 30% to 80% Sort Yield: Despite increasing complexity, rate of yield learning must improve in order to compensate for longer process cycle time in the future.



Wafer Environment Contamination Control

- **Purpose:**

- Define technology requirements for
 - cleanliness of process materials and
 - wafer environment
- Based on the findings and analyses of other roadmap sections
- In general there were minimal changes to this section from 1999 to 2001



Key Challenge

- ***Correlation of Impurity Level to Yield***
 - Methodology for determining the effects of trace impurities on device performance is needed now
 - Development of test structure to allow correlation of fluid/gas contamination types/levels to yield
 - Without correlations, difficult to predict need for increasing levels of process material purity
 - Without such predictions, IDMs run risk of not having the right materials/distribution systems available in conjunction with new processes and products
 - Lack of clear correlation between impurity levels and device performance has led either to
 - a direct relaxation of material impurity requirements or
 - the postponement of possible improvements



Table 95: Wafer Environment Contam. Control

Technology Requirements – Near Term

Table 95a Technology Requirements for Wafer Environmental Contamination Control—Near-term

YEAR OF PRODUCTION	2001 130nm	2002 115nm	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm
<i>Wafer Environment Control</i>							
Critical particle size (nm) [A]	65	58	52	45	38	35	33
# Particles > critical size (/m ³) [B]	5	4	3	2	2	1	1
<i>Airborne Molecular Contaminants (ppt) [C]</i>							
Lithography—bases (as amine, amide, or NH ₃)	750	750	750	750	750	<750	<750
Gate—metals (as Cu, E=2 × 10 ⁻⁵) [C]	0.2	0.2	0.15	0.1	0.1	0.07	<0.07
Gate—organics (as molecular weight greater than or equal to 250, E=1 × 10 ⁻³) [D]	100	90	80	70	60	60	50
Organics (as CH ₄)	1800	1620	1440	1260	1100	900	<900
Salicidation contact—acids (as Cl ⁻ , E=1 × 10 ⁻⁵)	10	10	10	10	10	<10	<10
Salicidation contact—bases (as NH ₃ , E=1 × 10 ⁻⁶)	20	16	12	10	8	4	<4
Dopants (P or B) [E]	<10	<10	<10	<10	<10	<10	<10
<i>Process Critical Materials</i>							
Critical particle size (nm) [A]	65	58	52	45	38	35	33



Table 95: Wafer Environment Contam. Control Technology Requirements – Near Term

YEAR OF PRODUCTION	2001 130nm	2002 115nm	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm
<i>Ultrapure Water</i>							
Total oxidizable carbon (ppb)	1	1	<1	<1	<1	<1	<1
Bacteria (CFU/liter)	<1	<1	<1	<1	<1	<1	<1
Total silica (ppb)	0.1	0.1	0.1	0.1	0.05	0.05	0.05
# Particles>critical size (/ml)	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
Critical cation, anion, metals (ppt, each)	<20	<20	<20	10	10	10	10
<i>Liquid Chemicals [F]</i>							
Particles—critical size (ml)	<10	<10	<10	<10	<1	<1	<1
HF-, H ₂ O ₂ , NH ₄ OH: Fe, Cu (ppt, each)	<150	<135	<110	<100	<90	<50	<50
Critical cation, anion, metals (ppt, each)	<10	<10	<10	<5	<5	<5	<1
HF-only, TOC (ppb)	<30	<30	<25	<20	<15	<10	<10
HCl, H ₂ SO ₄ : All impurities (ppt)	<1000	<1000	<1000	<1000	<1000	<1000	<1000
BEOL Solvents, Strippers K, Li, Na, (ppt, each)	<1000	<1000	<1000	<1000	<1000	<1000	<1000
<i>ILD CVD Precursors (e.g., TEOS)</i>							
Metals (ppb)	<1	<1	<1	<0.1	<0.1	<0.1	<0.1
H ₂ O (ppmV)	<10	<10	<10	<5	<5	<5	<1
<i>Bulk Gases</i>							
N ₂ , O ₂ , Ar, H ₂ : H ₂ O, O ₂ , CO ₂ , CH ₄ (ppt, each)	<1000	<1000	<1000	<1000	<1000	<100	<100
# Particles > critical size (/liter)	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1
<i>Specialty Gases</i>							
# POU particles > critical size (/liter) [F]	2	2	2	2	2	2	2
<i>Inerts—Oxide/Photoresist Etchants/Strippers</i>							
O ₂ (ppbV)	<1000	<1000	<1000	<500	<500	<500	<100
H ₂ O (ppbV)	<1000	<1000	<1000	<500	<500	<500	<100
Individual specified metals (ppbWT)	<10	<10	<10	<10	<10	<1	<1



Table 95: Wafer Environment Contam. Control

Technology Requirements – Long Term

Table 95b Technology Requirements for Wafer Environmental Contamination Control—Long-term

YEAR OF PRODUCTION	2010 45nm	2013 32nm	2016 22nm
<i>Wafer Environment Control</i>			
Critical particle size (nm) [A]	23	16	11
# Particles > critical size (/m ³) [B]	1	<1	<1
<i>Airborne Molecular Contaminants (ppt) [C]</i>			
Lithography—bases (as amine, amide, or NH ₃)	<750	<750	<750
Gate—metals (as Cu, E=2 × 10 ⁻⁵) [C]	<0.07	<0.07	<0.07
Gate—organics (as molecular weight greater than or equal to 250, E=1 × 10 ⁻³) [D]	40	30	20
Organics (as CH ₄)	<900	<900	<900
Salicidation contact—acids (as Cl ⁻ , E=1 × 10 ⁻⁵)	<10	<10	<10
Salicidation contact—bases (as NH ₃ , E=1 × 10 ⁻⁶)	<4	<4	<4
Dopants (P or B) [E]	<10	<10	<10
<i>Process Critical Materials</i>			
Critical particle size (nm) [A]	23	16	11



Table 95: Wafer Environment Contam. Control Technology Requirements – Long Term

YEAR OF PRODUCTION	2010 45nm	2013 32nm	2016 22nm
<i>Ultrapure Water</i>			
Total oxidizable carbon (ppb)	<1	<1	<1
Bacteria (CFU/liter)	<1	<1	<1
Total silica (ppb)	0.01	<0.01	<0.01
Particles—critical size (ml)	<0.2	<0.2	<0.2
Critical cation, anion, metals (ppt, each)	<10	<10	<10
<i>Liquid Chemicals [F]</i>			
# Particles > critical size (/ml)	<1	<1	<1
HF-, H ₂ O ₂ , NH ₄ OH: Fe, Cu (ppt, each)	<50	<40	<40
Critical cation, anion, metals (ppt, each)	<1	<1	<1
HF-only, TOC (ppb)	<8	<6	<4
HCl, H ₂ SO ₄ : All impurities (ppt)	<1000	<1000	<1000
BEOL Solvents, Strippers K, Li, Na, (ppt, each)	<1000	<1000	<1000
<i>ILD CVD Precursors (e.g., TEOS)</i>			
Metals (ppb)	<0.1	<0.1	<0.1
H ₂ O (ppmV)	<1	<1	<1
<i>Bulk Gases</i>			
N ₂ , O ₂ , Ar, H ₂ : H ₂ O, O ₂ , CO ₂ , CH ₄ (ppt, each)	<100	<100	<100
# Particles > critical size (/liter)	<0.1	<0.1	<0.1
<i>Specialty Gases</i>			
# POU particles > critical size (/liter) [F]	2	2	2
<i>Inerts—Oxide/Photoresist Etchants/Strippers</i>			
O ₂ (ppbV)	<100	<50	<50
H ₂ O (ppbV)	<100	<50	<50
Individual specified metals (ppbWT)	<1	<1	<1



Table 80: Wafer Environment Contam. Control

Test Methodology for Ultrapure Water

PARAMETER	MEASURED (POD/POC)	TEST METHOD
Resistivity	Online	Electric cell
Viable bacteria	Lab	Incubation
EPI Bacteria	Lab	Stained samples w/ Fluorescent Microscopy
Scan RDI	Lab	Laser-scanning Cytometry
TOC	Online	Resistivity / CO ₂
Reactive Silica	Online or Lab	Colormetric
Colloidal Silica	Calculation	Total minus Reactive
Total Silica	Lab	ICP/MS
Particle Monitoring	Online	Light scatter
Particle Count	Lab	SEM – Capture filter at various pore sizes
Cations, anions, metals	Lab	Ion chromatography, ICP/MS
Dissolved O ₂	Online	Electric Cell



ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- Foup Standard for wafer handling using PWP
 - **Resting in processing chamber**
 - **Need real conditions on test wafer**
- Coupling factor in yield model for defect budget is actually 2, not 5 as indicated in the current presentation of the YE Chapter.



ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- HARI - still most important YE challenge
 - SEMs
 - Improve COO
 - Alternative holographic solution
 - Current staffing in SEM Inspection
 - Methodology change
 - Test structures
 - Test structures with SEM
 - Tied to tool
 - Test structure development
 - Short loop tied to a particular company
 - Design into regular devices and scribe lane
 - cross discussion with design; not improved for 2 years



ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- JEITA – datamining of test and flow history
 - **6 month inventory**
 - **sampling too limited**
 - **make structure more sensitive by “attracting” particles**
 - **educated metrology to avoid additional (unwanted) defects**
- Yield Model and Defect Budget
 - **Big systematic yield problem if using Poisson model**
 - **Concentrate on difference in ramp-up phase (10-20% yield) and entitlement phase (75-80%)**
 - **50-60% yield targets are highly dependent on systematic loss.**
- Defect detection is more important than the model in making yield correlation



ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- Elemental analysis can be SPC'ed
 - **Topology and EDX composition**
 - **EDX classification**
- If we have limited detection (red brick wall), then all yield loss becomes systematic.
- Systematic yield loss
 - **Topology and EDX composition**
 - **EDX classification**
 - process marginalities
 - doping out of spec
 - design lay-out
 - edge



ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- JEITA Enquete (Inquiry of Japanese Semiconductor Manufacturers) – only defect control limit canvassed. Details given during ISSM 2002 –Tokyo, Kitajima-san of Work Group (WG) 11
- US Defect Inquiries – PWP data collected
- Must fold Defect Budget Models from ITRS and JEITA together
- JEITA – systematic yield loss is 10%
- Systematic yield loss termed “invisible defects”
- Osada-san presented a list of typical cause of yield loss – will request that he forward to me and all ITRS/Regional TWG members



ITRS Yield Enhancement TWG Meeting

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- How to incorporate systematic yield mathematically
 - Portion by step
 - Cp/Cpk loss
 - Should be based on vendor specs for performance (variation-what is yield impact?)
 - Yield priority
 - JEITA enquete
 - Include process stability; incorporation in yield model.
 - “Is” random table can be reduced by members
 - bScaled limits for yield targets
- Size of database incorporating systematic sources may be very large and require automated handling.



ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- JEITA WG 11 representatives for Enquete should come to US to talk about changes for 2003./European representatives can participate by teleconference.
- Manuela Huber to send to Osada-san full documentation of model/procedures from SEMATECH to/fm WG 11/then discussion.
- Technical requirements
 - **Cluster parameter = 2; will only slightly affect all budget figures except 130nm node.**
 - **Need real numbers.**
 - **More of a proportion budget.**
 - **Need separate vendor specification. – 2003**



ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- Detection for 2003b
 - Standardization of inspection locations in the flow.
 - Tool-to-tool matching – recommendations
 - Tool Matching for Inspection tools
 - Location
 - Sensitivity
 - Sizing – no current defect standards for SEMsb



ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- Detection for 2003b (continued)
 - **PSL spheres**
 - Need new standards (non-plastic)
 - Different materials
 - Si
 - SiN
 - SiO
 - Need patterned standards that are inexpensive
 - Standards for haze – background
 - SEM – gold on carbon
 - Resolution - NIST magnification standards
 - Daily check – about an hour
 - Include coordinate accuracy and tool matching
 - **Include haze requirements with methodology**
 - **Must also handle SOI/Haze/COPS**
 - Coordinate with Silicon Sub-TWG; Howard Huff



International Technology Roadmap for Semiconductors

24 July 2002 Work In Progress – Not for Publication

ITRS Yield Enhancement TWG Meeting

Erlangen, Germany - 10-11 April 2002

- Detection for 2003b (continued)
 - Need separation of certain wafer levels that are tough for defect detection.
 - We need “truthteller” time to establish a change in defect trend – 1 day to 4 weeks.
 - Excursion control should be established in production due to change in sampling. 10% sampling may not be good enough.
 - Need different learning rate following ramp.
 - Need separation of defect excursion and yield excursion
 - different emphasis in ramp and entitlement



Yield Model and Defect Budget

Technology Requirements:

- **Approach to define defect budget requirements:**
 - Input: results of 1997, 1999, 2000 surveys of current PWP and PID data at Intl. SEMATECH Member Companies.
 - For 2001 (130nm node) calculation is based on generic Intl. Sematech process flow, e.g. for logic:
 - **494 Processing Steps**
 - **25 Mask Levels**
 - **7 Cu Metal Layers**
 - Yield model used for PWP calculation per tool type:

$$Y_{sort} = Y_s * Y_r = Y_s * \left\{ \frac{1}{\left(1 + \frac{AD}{\alpha}\right)^\alpha} \right\}$$

Y_{sort} = Probe Yield

Y_s = Systematic Limited Yield

Y_r = Random Defect Limited Yield

A = critical Chip Area (m²)
(Stapper model)

D = Electrical Fault Density (/m²)
(includes kill ratio, transfer coefficient)

α = Cluster Factor (α=2)



International Technology Roadmap for Semiconductors

24 July 2002 Work In Progress – Not for Publication

Yield Model and Defect Budget

Technology Requirements:

- **Extrapolation for future technology node requirements:**

- from median PWP value for typical tool in each process module by considering increase in area, increase in complexity, and shrinking feature size.

$$PWP_n = PWP_{n-1} * \frac{F_n}{F_{n-1} \left(\frac{S_{n-1}}{S_n} \right)^2}$$

with:

PWP = Particles per Wafer pass (/m²)

n = Technology Node of Interest

F = Faults per Mask

S = Minimum Defect Size (nm)

- **Key assumption:**

- No new process, material, or tool will be acceptable with a larger PWP budget than prior processing methods.
- Defect budgeting method tends to be a worst case model since all process steps are assumed to be at minimum device geometry.
- Technology requirement color-code determined by tool yield impact partitioning study



International Technology Roadmap for Semiconductors

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