Overall Roadmap Technology Characteristics

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor clock rate, GHz**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

Overall Roadmap Technology Characteristics

Table B ITRS Table Structure—
Key Lithography-Related Characteristics by Product Type

Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**

Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**

Overall Roadmap Technology Characteristics

The *2001 ITRS* includes a correction of the past "rounding" convention for the technology node labels. The actual mathematical trend reduces the nodes by 50% every other node, resulting in an actual versus rounded node number targets, starting from 350 nm in 1995 as follows:

Table C Rounded versus Actual Trend Numbers

YEAR OF PRODUCTION	1995	1997	1999	2001	2004	2007	2010	2013	2016
Actual Trend Numbers (nm)	350	247.5	175	123.7	87.5	61.9	43.8	30.9	21.9
ITRS Rounded Node Numbers (nm)	350	250	180	130	90	65	45	32	22

Note the new "rounding" corrections become more critical as the industry moves into the double-digit technology nodes. Some regions, for past publication consistency, will continue to track the previous technology nodes beginning with 100 nm/2003, resulting in milestones that are placed one year earlier than the present 2001 roadmap convention (70 nm/2006; 50 nm/2009; 35nm/2012; 25 nm/2015).

Overall Roadmap Technology Characteristics

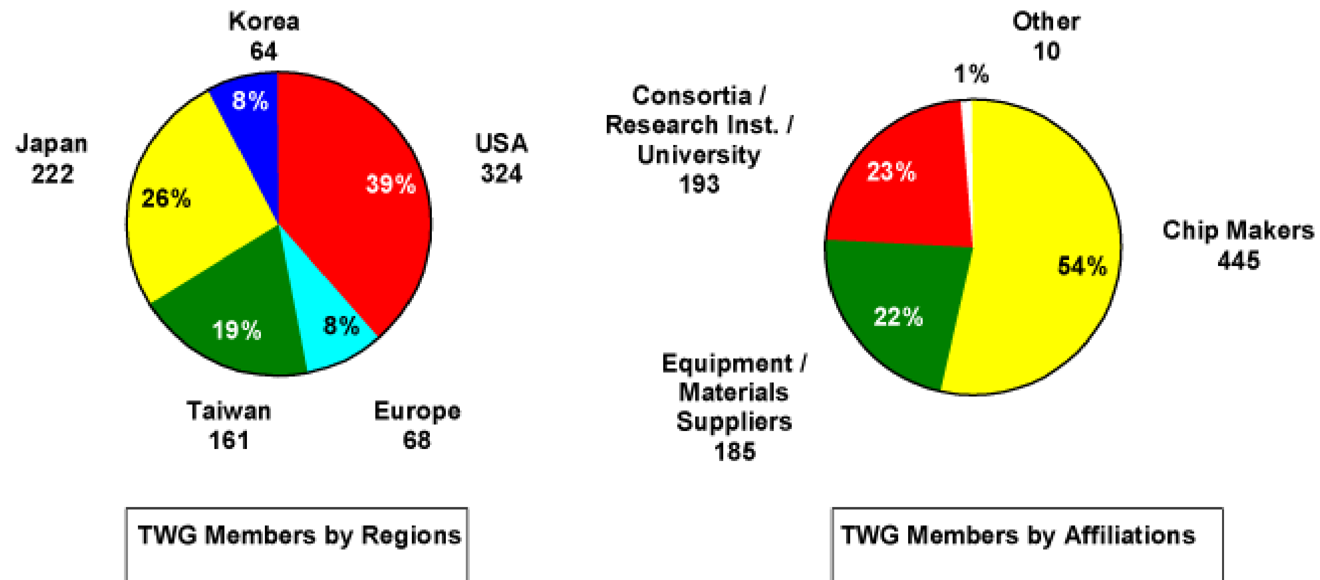


Figure 1 Composition of the Technology Working Group (TWG).

Overall Roadmap Technology Characteristics

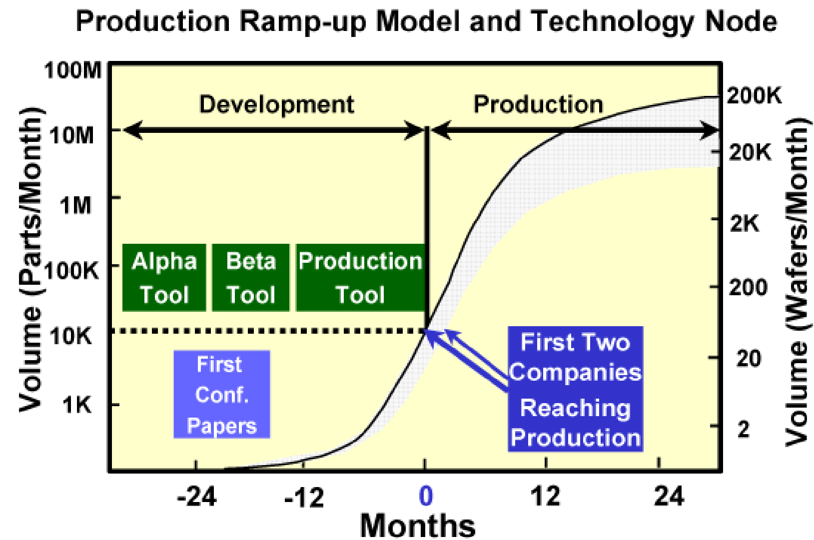


Figure 2 A Typical Production "Ramp" Curve

The "Production" time in ITRS refers to the time when the first company brings a technology to production and a second company follows within three months. It is noted that the ITRS Roadmap, by its definition, focuses on forecasting the earliest introduction of the leading-edge technologies in respective fields for producing semiconductors.

Note that some rows in the ORTC and technology requirements tables refer to other timing points, which are defined for each case (e.g., "at sample"). Of course, for the "Long-term Years," for which the table intervals are three years, it is possible for the "best-estimate year of production" to fall in between the selected three-year intervals for some technology requirements. Also note that the "production" ramp in Figure 2 can be viewed as the time to ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (wspm) capacity, the time to ramp from 20 wspm to full capacity can take 9–12 months. This time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month if the chip size were 140 mm^2 (430 gross die per 300 mm wafer × 20K wspm × 70% total yield from wafer starts to finished product = 6M units/month).

Overall Roadmap Technology Characteristics

It is obvious that many companies, for a variety of reasons, may choose to introduce a technology node later than the earliest introductions, hence that there is a wide variation of the technologies in actual production status from leading-edge to trailing-edge. Figure 3 shows, in horizontal bar-graph, the actual, annual worldwide wafer production capacity distributions over different process feature sizes. The distributions are quite wide-spread while the ITRS Technology Nodes, shown in small blue marks, are located exactly on the leading-edges of each of them.

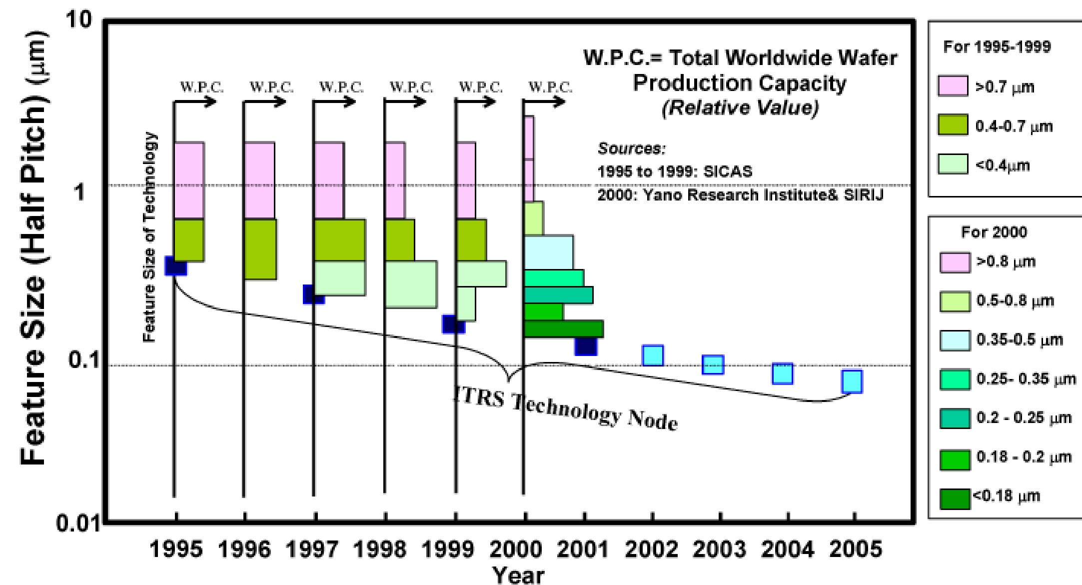
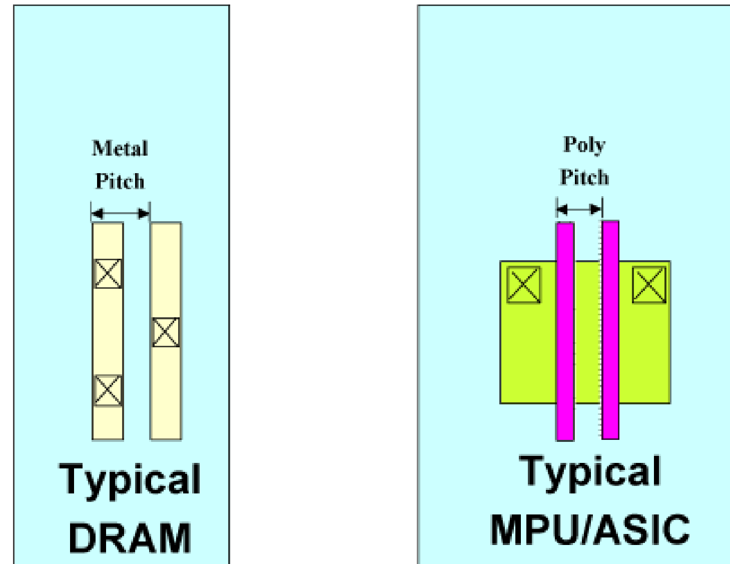


Figure 3 Technology Node Compared to
Actual Production Capacity Technology Distribution

Overall Roadmap Technology Characteristics



** DRAM pitch determines the technology "node" designation*

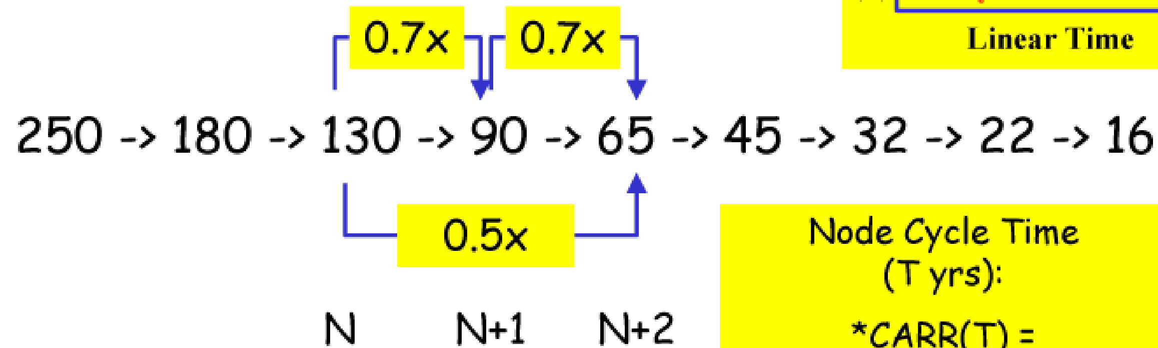
Figure 4 Definition of the Half Pitch and Gate Length

MOS Transistor Scaling
(1974 to present)

S=0.7

[0.5x per 2 nodes]

Figure 5 MOS Transistor Scaling—1974 to present



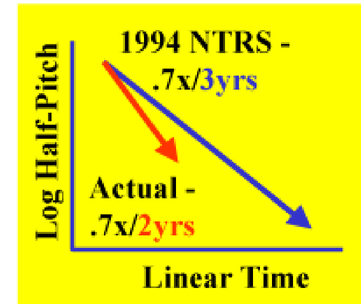


Figure 6 Scaling Calculator

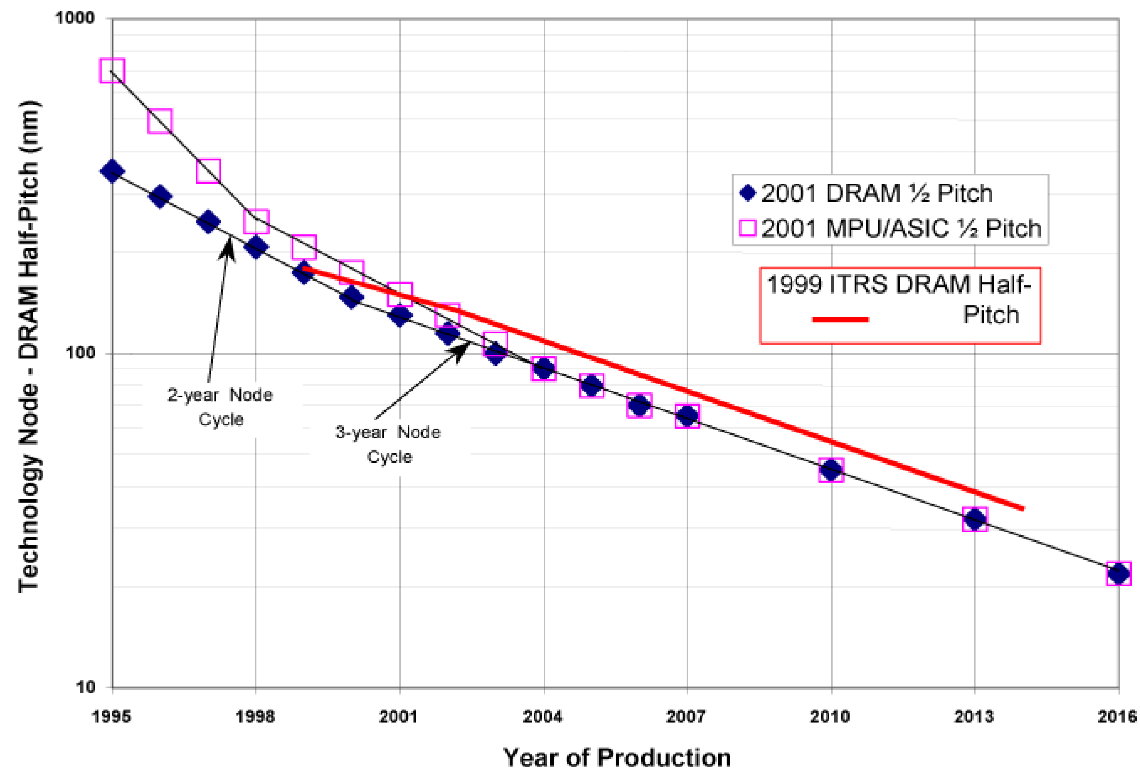


Figure 7 ITRS Roadmap Acceleration Continues—Half Pitch Trends

Overall Roadmap Technology Characteristics

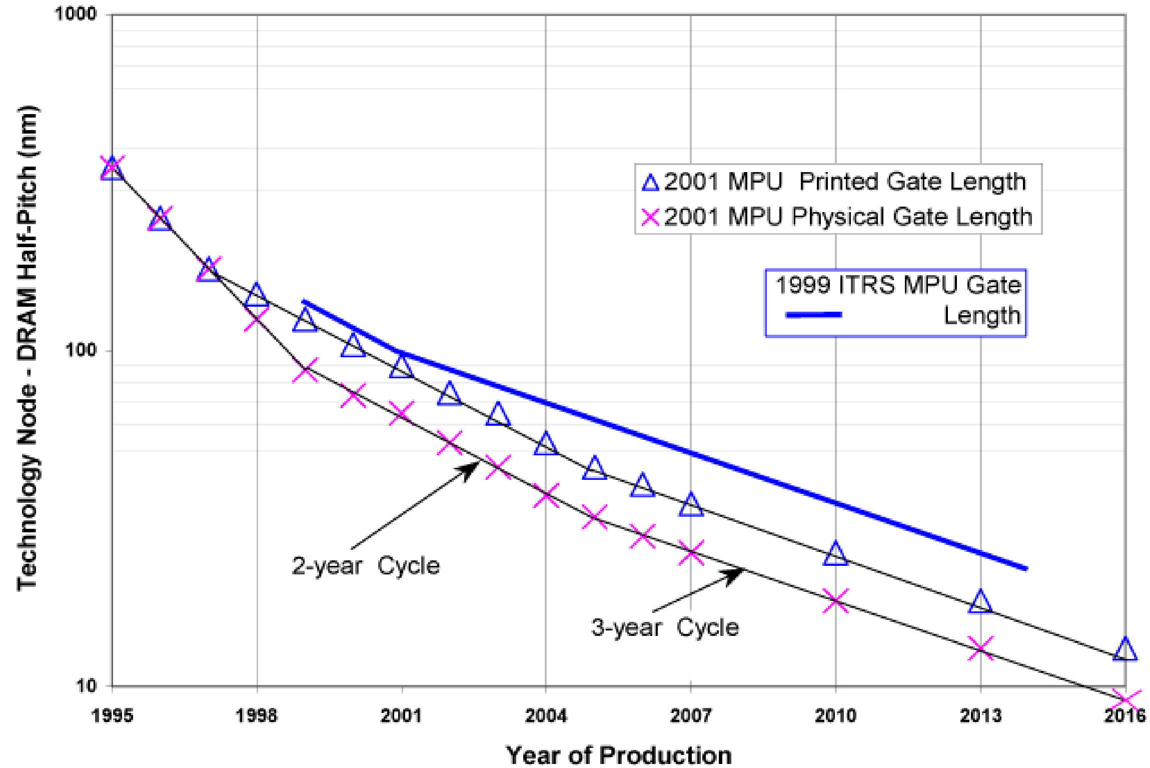


Figure 8 ITRS Roadmap Acceleration Continues—Gate Length Trends

Overall Roadmap Technology Characteristics

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm) ††	90	75	65	53	45	40	35
MPU Physical Gate Length) (nm)	65	53	45	37	32	28	25
ASIC/Low Power Printed Gate Length (nm) ††	130	107	90	75	65	53	45
ASIC/Low Power Physical Gate Length) (nm)	90	75	65	53	45	37	32

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm) ††	25	18	13
MPU Physical Gate Length) (nm)	18	13	9
ASIC/Low Power Printed Gate Length (nm) ††	32	22	16
ASIC/Low Power Physical Gate Length) (nm)	22	16	11

Notes for Tables 1a and 1b:

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "Physical" gate lengths may be reduced from the "as-printed" dimension. These "Physical" gate-length targets are driven by the need for maximum speed performance in logic Microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design ITWG Tables as needs that drive device design and process technology requirements.

Table 1c DRAM Production Product Generations and Chip Size Model—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Cell area factor [a]	8	8	6	6	6	6	6
Cell area [Ca = af²] (μm²)	0.130	0.103	0.061	0.049	0.039	0.031	0.024
Cell array area at production (% of chip size) §	54.8%	55.3%	55.7%	56.1%	56.4%	56.7%	57.0%
Generation at production §	512M	512M	1G	1G	2G	2G	4G
Functions per chip (Gbits)	0.54	0.54	1.07	1.07	2.15	2.15	4.29
Chip size at production (mm²)§	127	100	118	93	147	116	183
Gbits/cm² at production §	0.42	0.54	0.91	1.15	1.46	1.85	2.35

Table 1d DRAM Production Product Generations and Chip Size Model—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Cell area factor [a]	6	4	4
Cell area [Ca = af²] (μm²)	0.012	0.004	0.002
Cell array area at production (% of chip size) §	57.7%	58.1%	58.4%
Generation at production §	8G	32G	64G
Functions per chip (Gbits)	8.59	34.36	68.72
Chip size at production (mm²)§	181	239	238
Gbits/cm² at production §	4.75	14.35	28.85

Notes for Tables 1c and 1d:

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows: 1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

1. ***at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and***
2. ***at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).***

InTER-generation chip size growth rate varies to maintain one chip per 572mm² field at Introduction and two chips per 572mm² field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Cell area factor [a]	8	8	6	6	6	6	6
Cell area [$Ca = af^2$] (μm^2)	0.130	0.103	0.061	0.049	0.039	0.031	0.024
Cell array area at introduction (% of chip size) §	71.3%	71.8%	72.2%	72.6%	72.9%	73.2%	73.5%
Generation at introduction §	2G	2G	4G	4G	8G	8G	16G
Functions per chip (Gbits)	2.15	2.15	4.29	4.29	8.59	8.59	17.18
Chip size at introduction (mm^2) §	390	308	364	287	454	359	568
Gbits/cm^2 at introduction §	0.55	0.70	1.18	1.49	1.89	2.39	3.03

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years

Year of Production	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Cell area factor [a]	6	4	4
Cell area [$Ca = af^2$] (μm^2)	0.012	0.004	0.002
Cell array area at introduction (% of chip size) §	74.2%	74.6%	74.9%
Generation at introduction §	32G	64G	64G
Functions per chip (Gbits)	34.36	68.72	68.72
Chip size at introduction (mm^2) §	563	373	186
Gbits/cm^2 at introduction §	6.10	18.42	37.00

Notes for Tables 1e and 1f:

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows:

1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

1. ***at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and***
2. ***at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).***

InTER-generation chip size growth rate varies to maintain one chip per 572mm² field at Introduction and two chips per 572mm² field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
SRAM Cell (6-transistor) Area factor ++	126.1	123.0	120.3	117.8	115.6	113.7	111.9
Logic Gate (4-transistor) Area factor ++	320.0	320.0	320.0	320.0	320.0	320.0	320.0
SRAM Cell (6-transistor) Area efficiency ++	0.63	0.63	0.63	0.63	0.63	0.63	0.63
Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50	0.50	0.50	0.50	0.50
SRAM Cell (6-transistor) Area w/overhead ++	3.3	2.5	2.0	1.5	1.2	0.93	0.73
Logic Gate (4-transistor) Area w/overhead ++	10.4	8.2	6.5	5.2	4.1	3.3	2.6
Transistor density SRAM (Mtransistors/cm^2)	184	237	305	393	504	646	827
Transistor density logic (Mtransistors/cm^2)	38.6	48.6	61.2	77.2	97.2	122.5	154.3
Generation at introduction *	p04c	—	—	p07c	—	—	p10c
Functions per chip at introduction (million transistors [Mtransistors])	193	243	307	386	487	614	773
Chip size at introduction (mm^2) ‡	280	280	280	280	280	280	280
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	69	87	110	138	174	219	276
Generation at production *	p01c	—	—	p04c	—	—	p07c
Functions per chip at production (million transistors [Mtransistors])	97	122	153	193	243	307	386
Chip size at production (mm^2) §§	140	140	140	140	140	140	140
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	69.0	87.0	109.6	138.0	173.9	219.1	276.1

Notes for Tables 1g and 1h:

++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

**** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p01c, was introduced in 1999, but not ramped into volume production until 2001; similarly, the p04c, is introduced in 2001, but is targeted for volume production in 2004.***

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/1999), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5× every two-year technology node through 2001, then 0.5× every three-year technology node after 2001.

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
SRAM Cell (6-transistor) Area factor ++	107.8	106.7	105.7
Logic Gate (4-transistor) Area factor ++	320.0	320.0	320.0
SRAM Cell (6-transistor) Area efficiency ++	0.63	0.63	0.63
Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50
SRAM Cell (6-transistor) Area w/overhead ++	0.22	0.17	0.13
Logic Gate (4-transistor) Area w/overhead ++	0.82	0.65	0.51
Transistor density SRAM (Mtransistors/cm^2)	1718	3532	7208
Transistor density logic (Mtransistors/cm^2)	309	617	1235
Generation at introduction *	p13c	p16c	p19c
Functions per chip at introduction (million transistors [Mtransistors])	1546	3092	6184
Chip size at introduction (mm^2) ‡	280	280	280
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	552	1104	2209
Generation at production *	p10c	p13c	p16c
Functions per chip at production (million transistors [Mtransistors])	773	1546	3092
Chip size at production (mm^2) §§	140	140	140
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	552	1104	2209

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Logic (Low-volume Microprocessor) High-performance ‡							
Generation at production **	p01h	—	p03h	—	p05h	—	p07h
Functions per chip (million transistors)	276	348	439	553	697	878	1106
Chip size at production (mm^2) §§	310	310	310	310	310	310	310
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	89	112	142	178	225	283	357
ASIC							
ASIC usable Mtransistors/cm^2 (auto layout)	89	112	142	178	225	283	357
ASIC max chip size at production (mm^2) (maximum lithographic field size)	800	800	572	572	572	572	572
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	714	899	810	1020	1286	1620	2041

Notes for Tables 1i and 1j:

**** p is processor, numerals reflect year of production; h indicates high-performance product. Examples—the high-performance processor, p99h, was ramped into volume production in 1999; similarly, the p01h, is introduced in 2001.**

‡ MPU High-performance Model—High-performance MPU includes large L2 and L3 on-chip SRAM (2MByte/1999) plus a larger logic core (P99h core = 25M transistor (Mtransistors) both SRAM and Logic functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5x every two-year technology node through 2001, then 0.5x every three-year technology node after 2001.

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Logic (Low-volume Microprocessor) High-performance ‡			
Generation at production **	—	p13h	—
Functions per chip (million transistors)	2212	4424	8848
Chip size at production (mm^2) §§	310	310	310
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	714	1427	2854
ASIC			
ASIC usable Mtransistors/cm^2 (auto layout)	714	1427	2854
ASIC maximum chip size at production (mm^2)(maximum lithographic field size)	572	572	572
ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4081	8163	16326

Notes for Tables 1i and 1j:

***** p is processor, numerals reflect year of production; h indicates high-performance product. Examples—the high-performance processor, p99h, was ramped into volume production in 1999; similarly, the p01h, is introduced in 2001.***

‡ MPU High-performance Model—High-performance MPU includes large L2 and L3 on-chip SRAM (2MByte/1999) plus a larger logic core (P99h core = 25M transistor (Mtransistors) both SRAM and Logic functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5x every two-year technology node through 2001, then 0.5x every three-year technology node after 2001.

Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

(Note: 2001 Lithographic field sizes represent current capability)

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length(nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Lithography Field Size							
Lithography Field Size—area (mm^2)	**800**	**800**	**800**	**800**	**800**	**800**	**572**
Lithographic field size — length (mm)	**32**	**32**	**32**	**32**	**32**	**32**	**26**
Lithographic field size — width (mm)	**25**	**25**	**25**	**25**	**25**	**25**	**22**
Maximum Substrate Diameter (mm) — High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	**300**	**300**	**300**	**300**	**300**	**300**	**300**

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years

Year of Production	2010	2013	2016
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Lithography Field Size			
Maximum lithographic field size—area (mm^2)			
Lithography Field Size—area (mm^2)	**572**	**572**	**572**
Maximum lithographic field size—length (mm)	**26**	**26**	**26**
Maximum lithographic field size—width (mm)	**22**	**22**	**22**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)			
Bulk or epitaxial or SOI wafer	**300**	**450**	**450**

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Number of Chip I/Os (Number of Total Chip Pads) — Maximum							
Total pads—MPU	**3072**	**3072**	**3072**	**3072**	**3072**	**3072**	**3072**
Signal I/O—MPU (1/3 of total pads)	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**
Power and ground pads—MPU (2/3 of total pads)	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**
Total pads—ASIC high-performance	**3000**	**3200**	**3400**	**3600**	**4000**	**4200**	**4400**
Signal I/O pads—ASIC high-performance	**1500**	**1600**	**1700**	**1800**	**2000**	**2100**	**2200**
Power and ground pads—ASIC high-performance (½ of total pads)	**1500**	**1600**	**1700**	**1800**	**2000**	**2100**	**2200**
Number of Total Package Pins—Maximum [1]							
Microprocessor/controller, cost-performance	**480–1,200**	**480–1320**	**500–1452**	**500–1600**	**550–1760**	**550–1936**	**600–2140**
Microprocessor/controller, high-performance	**1200**	**1320**	**1452**	**1,600**	**1,760**	**1,936**	**2,140**
ASIC (high-performance)	**1700**	**1870**	**2057**	**2263**	**2489**	**2738**	**3012**

Notes for Tables 3a and 3b:

[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by PWB technology and system cost.

The highest pin count applications will as a result use larger pitches and larger package sizes.

The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2:1 to 1:4

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Number of Chip I/Os (Number of Total Chip Pads) — Maximum			
Total pads—MPU	3840	4224	4416
Signal I/O—MPU (1/3 of total pads)	1280	1408	1472
Power and ground pads—MPU (2/3 of total pads)	2560	2816	2944
Total pads—ASIC high-performance	4800	5400	6000
Signal I/O pads—ASIC high-performance	2400	2700	3000
Power and ground pads—ASIC high-performance (½ of total pads)	2400	2700	3000
Number of Total Package Pins—Maximum [1]			
Microprocessor/controller, cost-performance	780–2782	1014–3616	1318–4702
Microprocessor/controller, high-performance	2782	3616	4702
ASIC (high-performance)	4009	5335	7100

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Chip Pad Pitch (micron)							
Pad pitch—ball bond	45	35	30	25	20	20	20
Pad pitch—wedge bond	40	35	30	25	20	20	20
Pad Pitch—area array flip-chip (cost-performance, high-performance)	160	160	150	150	130	130	120
Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	150	130	120	110	100	90	80
Cost-Per-Pin							
Package cost (cents/pin) (cost-performance)—minimum–maximum	0.80–1.60	0.75–1.44	0.70–1.30	0.66–1.17	0.61–1.06	0.56–1.03	0.64–1.00
Package cost (cents/pin) (Memory)—minimum–maximum	0.36–1.54	0.34–1.39	0.32–1.26	0.30–1.14	0.28–1.03	0.27–0.93	0.27–0.84

Table 4b Performance and Package Chips: Pads, Cost—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Chip Pad Pitch (micron)			
Pad pitch—ball bond	20	20	20
Pad Pitch—wedge bond	20	20	20
Pad Pitch—area array (cost-performance, high-performance)	90	80	70
Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	60	45	30
Cost-Per-Pin			
Package cost (cents/pin) (cost-performance)— minimum–maximum	0.49–0.98	0.42–0.93	0.36–0.79
Package cost (cents/pin) (Memory)— minimum–maximum	0.22–0.54	0.19–0.39	0.19–0.33

Table 4c Performance and Package Chips: Frequency On-Chip Wiring Levels—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Chip Frequency (MHz)							
On-chip local clock	1,684	2,317	3,088	3,990	5,173	5,631	6,739
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	1,684	2,317	3,088	3,990	5,173	5,631	6,739
Maximum number wiring levels—maximum	7	8	8	8	9	9	9
Maximum number wiring levels—minimum	7	7	8	8	8	9	9

Table 4d Performance and Package Chips: Frequency, On-Chip Wiring Levels—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Chip Frequency (MHz)			
On-chip local clock	11,511	19,348	28,751
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	11,511	19,348	28,751
Maximum number wiring levels—maximum	10	10	10
Maximum number wiring levels—minimum	9	9	10

Note for Tables 4c and 4d:

[1] The off chip frequency is expected to increase for a small number of high speed pins which will be used in combination with a large number of lower speed pins

[2] In 2001, high-speed serial communications transceiver devices are achieving chip-board frequencies of 3.125 GHz using CMOS, and 10 GHz using SiGe. In 2002 it is expected that 10 GHz transceivers will be fabricated using CMOS. 40 GHz SiGe devices are expected in 2003. The roadmap for higher levels of integration with wider bus widths, is shown in the High Frequency Serial Communications section in the Test chapter.

Table 5a Electrical Defects—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	**1,963**	**2,493**	**2,148**	**2,748**	**1,752**	**2236**	**1426**
MPU Random Defect D_0 at production chip size and 83% yield (faults/m^2) §§	**1,356**	**1,356**	**1,356**	**1,356**	**1,356**	**1,356**	**1,356**
# Mask Levels – MPU	**25**	**25**	**25**	**25**	**25**	**27**	**27**
# Mask Levels – DRAM	**21**	**22**	**24**	**24**	**24**	**24**	**24**

Table 5b Electrical Defects—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	**1356**	**1356**	**1356**
MPU Random Defect D_0 at production chip size and 83% yield (faults/m^2) §§	**1464**	**1116**	**1134**
# Mask Levels – MPU	**27**	**29**	**29**
# Mask Levels – DRAM	**26**	**26**	**26**

Notes for Tables 5a and 5b:

D_0 — defect density

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows:

1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

1. ***at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and***
2. ***at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).***

InTER-generation chip size growth rate varies to maintain one chip per 572mm² field at Introduction and two chips per 572mm² field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5× every two-year technology node through 2001, then 0.5× every three-year technology node after 2001.

Table 6a Power Supply and Power Dissipation—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Power Supply Voltage (V)							
V_{dd} (high performance)	1.1	1.0	1.0	1	0.9	0.9	0.7
V_{dd} (Low Operating Power, high V_{dd} transistors)	1.2	1.2	1.1	1.1	1.0	1.0	0.9
V_{dd} (Low Standby Power, high V_{dd} transistors)	1.2	1.2	1.2	1.2	1.2	1.2	1.1
Allowable Maximum Power [1]							
High-performance with heatsink (W)	130	140	150	160	170	180	190
Cost-performance (W)	61	75	81	85	92	98	104
Battery (W)—(hand-held)	2.4	2.6	2.8	3.2	3.2	3.5	3.5

Table 6b Power Supply and Power Dissipation—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Power Supply Voltage (V)			
V_{dd} (high performance)	0.6	0.5	0.4
V_{dd} (Low Operating Power, high V_{dd} transistors)	0.8	0.7	0.6
V_{dd} (Low Standby Power, high V_{dd} transistors)	1.0	0.9	0.9
Allowable Maximum Power [1]			
High-performance with heatsink (W)	218	251	288
Cost-performance (W)	120	138	158
Battery (W)—(hand-held)	3.0	3.0	3.0

Note for Table 6a and 6b:

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 7a Cost—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	21	14.8	10.5	7.4	5.3	3.7	2.6
DRAM cost/bit at (packaged microcents) at production §	7.7	5.4	3.8	2.7	1.9	1.4	0.96
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	176	124	88	62	44	31	22
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	107	75	53	38	27	19	13.3
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	97	69	49	34	24	17	12
Cost-Per-Pin							
Test Cost							
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	4.0	3.0	3.0	3.0	3.0	3.0	3.0
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Notes for Tables 7a and 7b:

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two-four years after introduction).

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows:
1999–2002/8×; 2003–2010/6×; 2011–2016/4×.
DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and
2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

InTER-generation chip size growth rate varies to maintain one chip per 572mm^2 field at Introduction and two chips per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.
Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5× every two-year technology node through 2001, then 0.5× every three-year technology node after 2001.

Table 7b Cost—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Affordable Cost per Function ++			
DRAM cost/bit (packaged microcents) at samples/introduction	0.93	0.33	0.12
DRAM cost/bit (packaged microcents) at production §	0.34	0.12	0.042
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78	2.75	0.97
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71	1.66	0.59
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.31	1.52	0.54
Cost-Per-Pin			
Test Cost			
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	4	4	4
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	2	3	4