

# Challenges and Opportunities for Achieving a Low-Power CMOS

Low Power → LOW  $V_{DD}$

Any Fluctuation degrades LSI Performance. S/N > 23 is required.

$$\text{Total Fluctuation } N: N = \sqrt{V_{1/f}^2 + V_{\sqrt{n}}^2 + V_{\sigma}^2}$$

$V_{1/f}$  : Flicker Noise

$V_{\sqrt{n}}$  : Quantum Noise

$V_{\sigma}$  : Threshold Voltage Fluctuation

$\text{Si}_3\text{N}_4$  gate insulator & (110)-surface-orientation CMOS

10 times larger current drivability

Signal Propagation Velocity along with Interconnect is completely

different from  $\frac{c}{\sqrt{\epsilon_r}}$  (c: Light Velocity,  $\epsilon_r$ : dielectric constant)

Propagation velocity slows down in LSI interconnect.

# The size and atomic scale expression of a MOS device

**Low Power Consumption → Low  $V_{DD}$**

Generation	0.18 $\mu\text{m}$	0.10 $\mu\text{m}$	0.05 $\mu\text{m}$	0.035 $\mu\text{m}$	0.025 $\mu\text{m}$
Effective Gate Oxide thickness $T_{\text{eff}}$	2.2 nm	1.25 nm	0.7 nm	0.55 nm	0.45 nm
Gate insulator film ( $\epsilon_r$ )	SiO <sub>2</sub> (3.9)	Si <sub>3</sub> N <sub>4</sub> (7.9)	HfO <sub>2</sub> (30)	HfO <sub>2</sub> (30)	HfO <sub>2</sub> (30)
Gate insulator film thickness $T_{\text{phy}}$	2.2 nm	2.53 nm	5.38 nm	4.23 nm	3.46 nm
Channel impurities concentration $N_A$	$2 \times 10^{18} \text{ cm}^{-3}$	$4 \times 10^{18} \text{ cm}^{-3}$	$1.4 \times 10^{19} \text{ cm}^{-3}$	$3 \times 10^{19} \text{ cm}^{-3}$	$6 \times 10^{19} \text{ cm}^{-3}$
Power supply voltage $V_{DD}$	1.7 V	1.1 V	0.6 V	0.5 V	0.4 V
Required $\sigma$ (threshold voltage variation) for $S/N$ or $S/\sigma > 23$	<b>74mV</b>	<b>48mV</b>	<b>26mV</b>	<b>22mV</b>	<b>17mV</b>
The number of atoms toward the gate length direction*	663	368	184	129	92
The number of atoms toward the gate insulator film thickness direction*	8	9	19	15	12
The number of impurity-atoms in a channel domain $n_a$	787	347	165	119	86
The number variation of impurity- atoms $sn_a = n_a$	28	18	12	10	9

\*The number of atoms was standardized based on the distance (0.27nm) between 2 atoms of Si crystal.

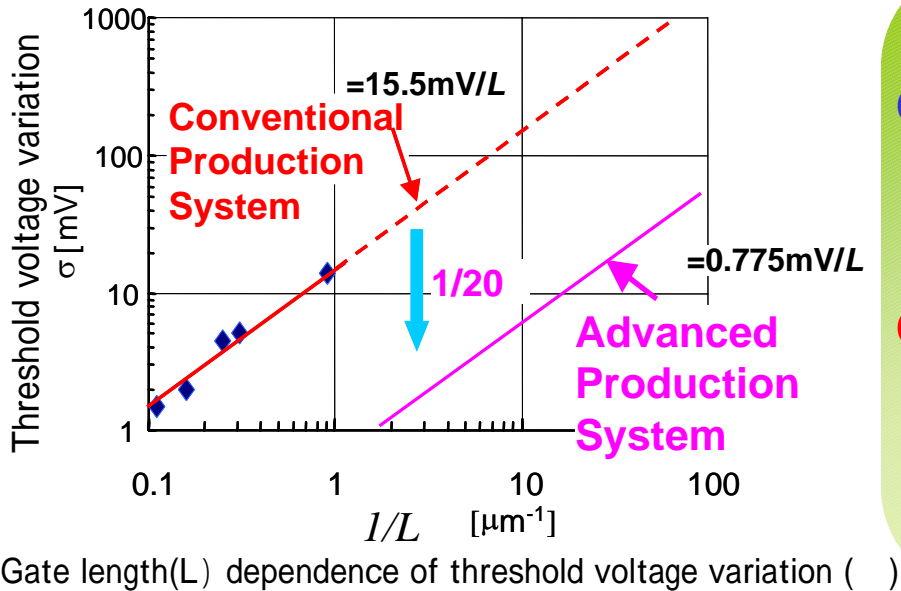
**Any fluctuation degrades LSI performance.**

***$S/N, S/\sigma > 23$  is required for prospective high speed MPU***

# Degradation of S/N by the threshold voltage variation accompanied by the device scaling

*S/N, S/σ > 23 is required*

*The case of W=L*



**Conventional Production System :  $\sigma = 15.5/L$  (1)**

*(in the case of W=L)*  
 0.1  $\mu\text{m}$  generation ( $L=0.1\mu\text{m}$ )  $\sigma = 155\text{mV}$  from Eqn.(1)

Power supply voltage  $V_{DD}=1.1\text{V}$

$$S/N = \frac{1.1\text{V}}{155\text{mV}} = 7.1$$



0.035  $\mu\text{m}$  generation ( $L=0.035\mu\text{m}$ )  $\sigma = 443\text{mV}$  from Eqn.(1)

Power supply voltage  $V_{DD}=0.5\text{V}$

$$S/N = \frac{0.5\text{V}}{443\text{mV}} = 1.1$$

**S/N degrades to 1/7**

**Advanced Production System :  $\sigma = 0.85/L$  (2)** *(in the case of W=L)*

**Threshold voltage variation: 1/20 of conventional production system**

0.1  $\mu\text{m}$  generation ( $L=0.1\mu\text{m}$ )  $\sigma = 7.75\text{mV}$  from Eqn.(2)

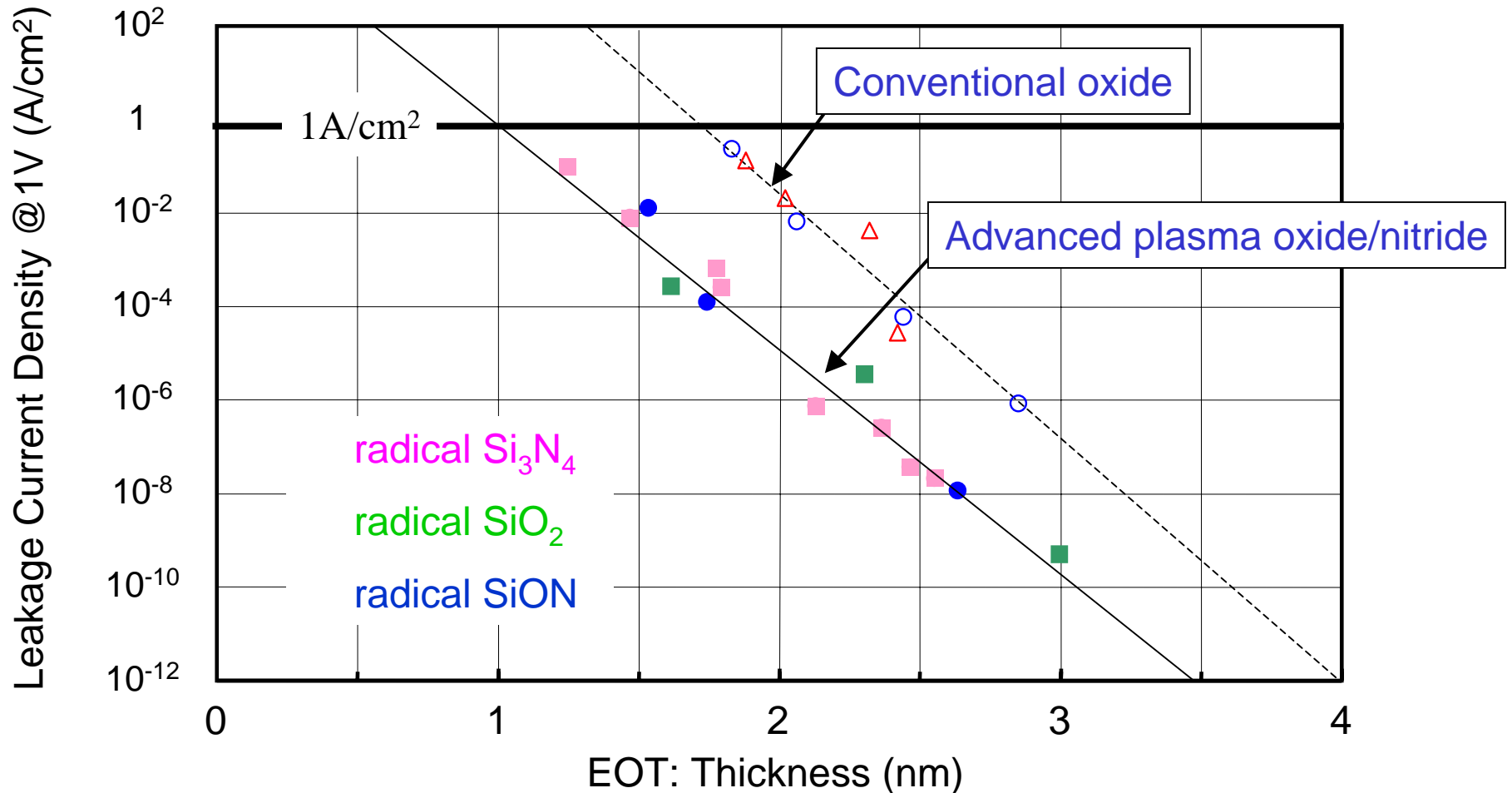
$$V_{DD}=1.1\text{V} \quad S/N = \frac{1.1\text{V}}{7.75\text{mV}} = 141$$

0.035  $\mu\text{m}$  generation ( $L=0.035\mu\text{m}$ )  $\sigma = 22.1\text{mV}$  from Eqn.(2)

$$V_{DD}=500\text{mV} \quad S/N = \frac{0.5\text{V}}{22.1\text{mV}} = 23$$

**S/N still be kept greater than 23 even in 0.035  $\mu\text{m}$  generation**

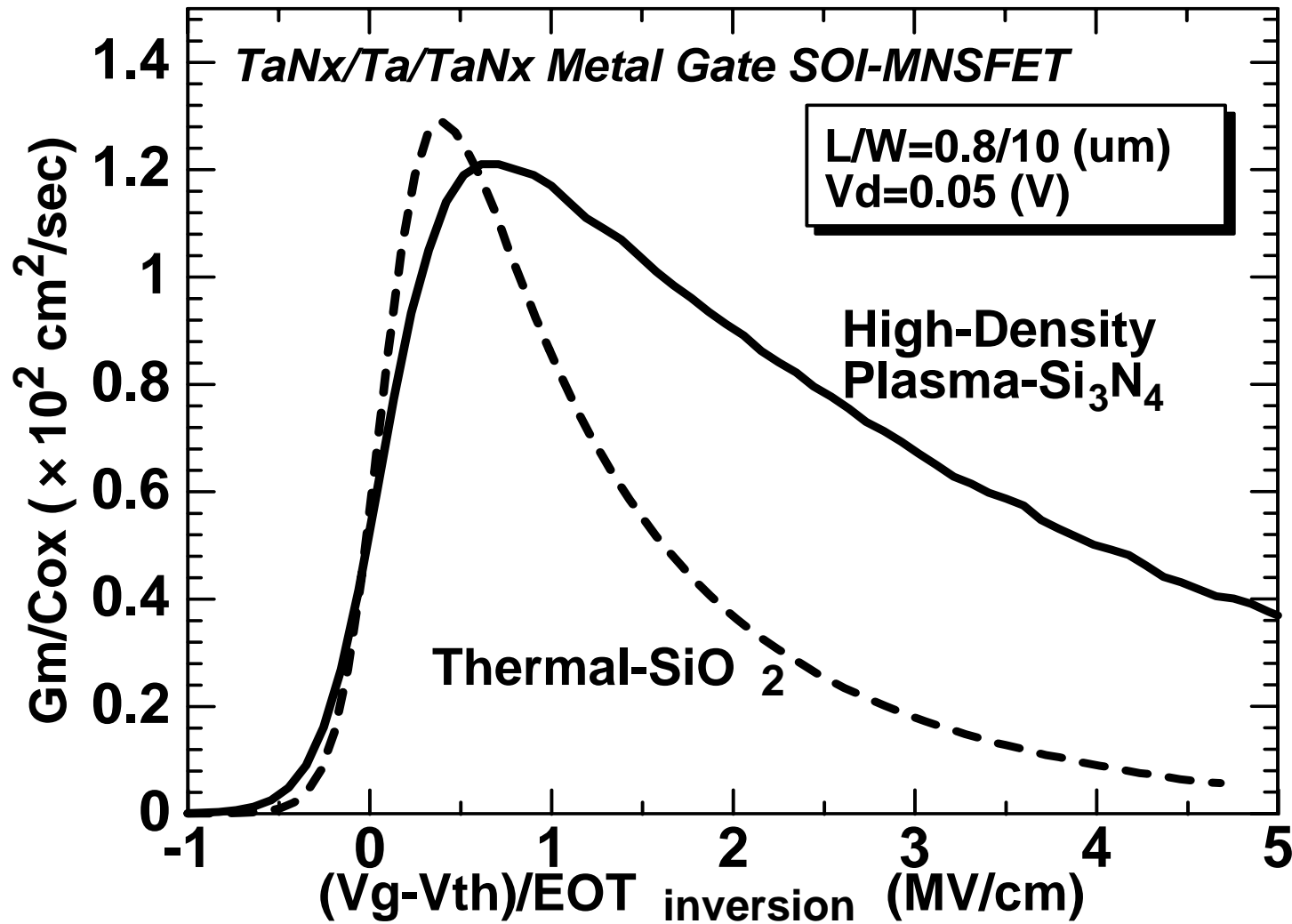
## Leakage Current (@1.0V) as a function of Oxide Thickness



**Si<sub>3</sub>N<sub>4</sub> (~4 times) Gate Insulator & (110) surface orientation (~ 2.5 times)**

**➔ 1/10 of Conventional Device Power Consumption**

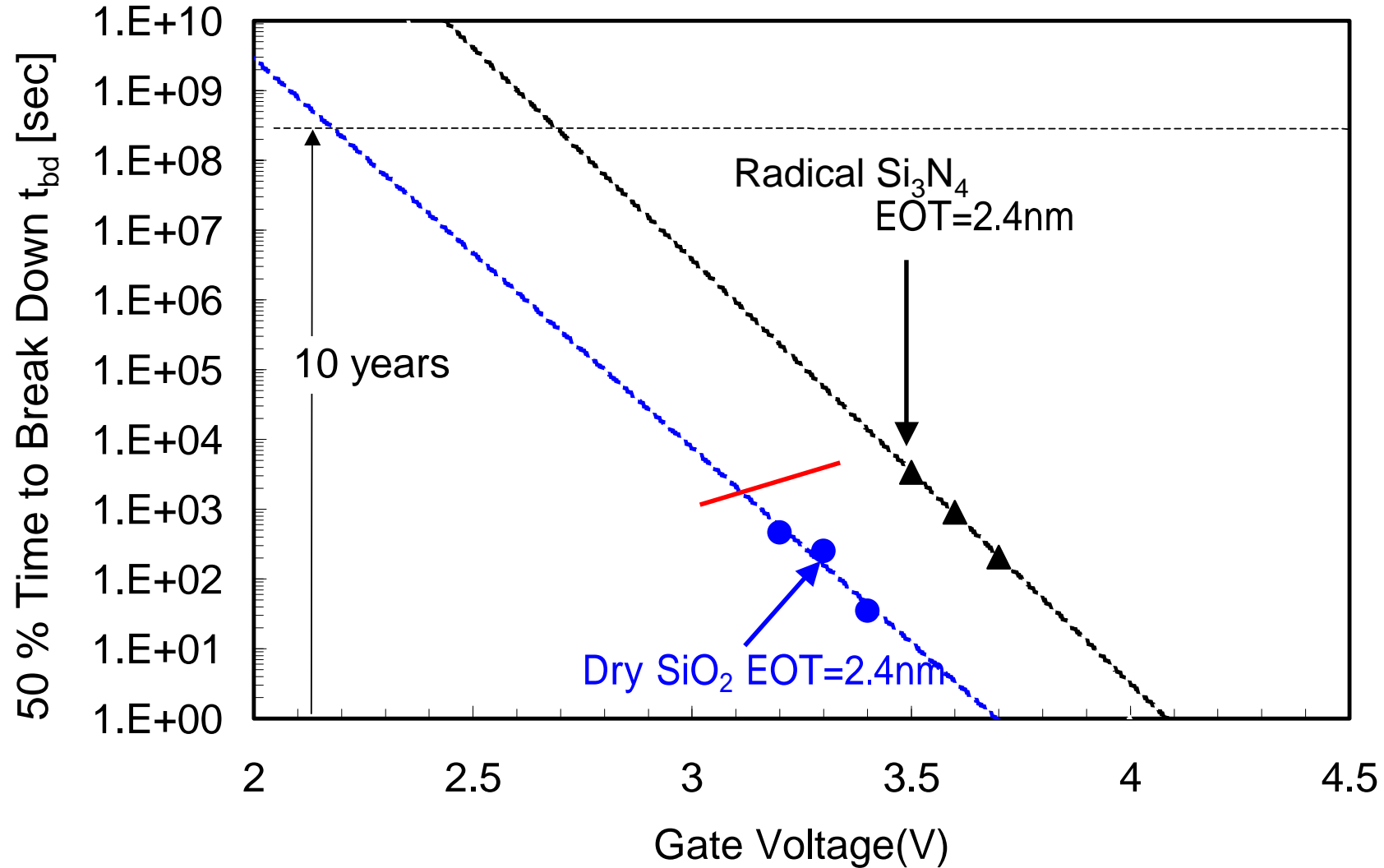
# Comparison of Transconductance



**Si<sub>3</sub>N<sub>4</sub> (~4 times) Gate Insulator & (110) surface orientation (~ 2.5 times)**

**➔ 1/10 of Conventional Device Power Consumption**

# 10 Year Lifetime Projection for $\text{Si}_3\text{N}_4$



**20~30% higher gate voltage can be applied to the  $\text{Si}_3\text{N}_4$  gate insulator  
2 times larger current drivability is available.**

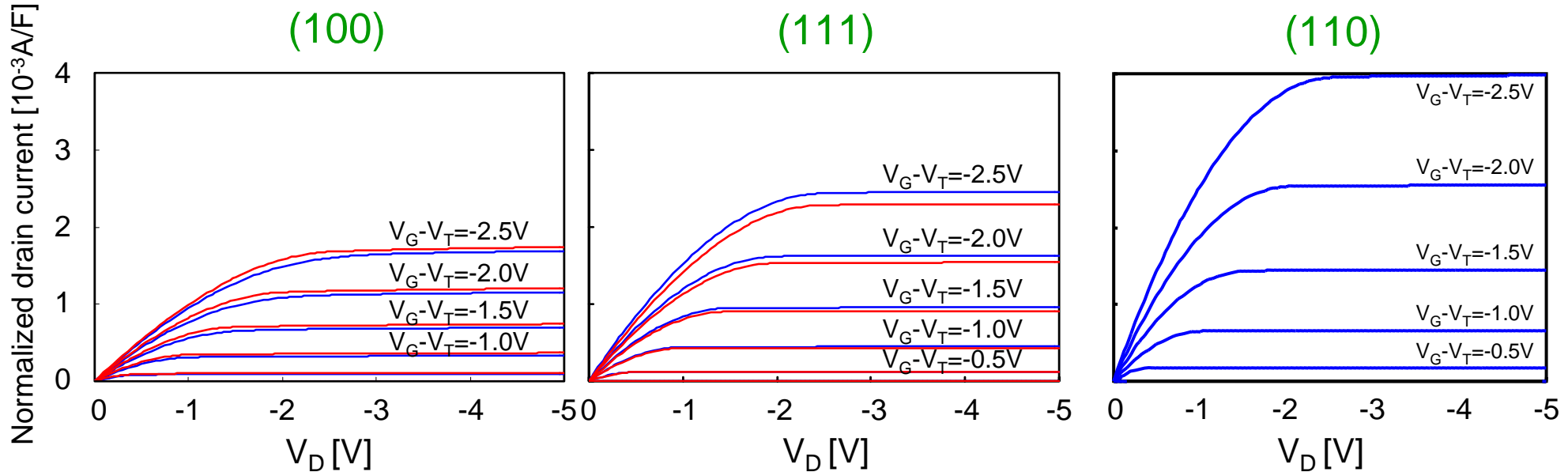
# Implement the (110)-oriented MOSFET

## -- Current drivability of pMOSFET --

(100):  $L=10\mu\text{m}$ ,  $W=50\mu\text{m}$

(111), (110):  $L=10\mu\text{m}$ ,  $W=300\mu\text{m}$

— Dry  
— O\*

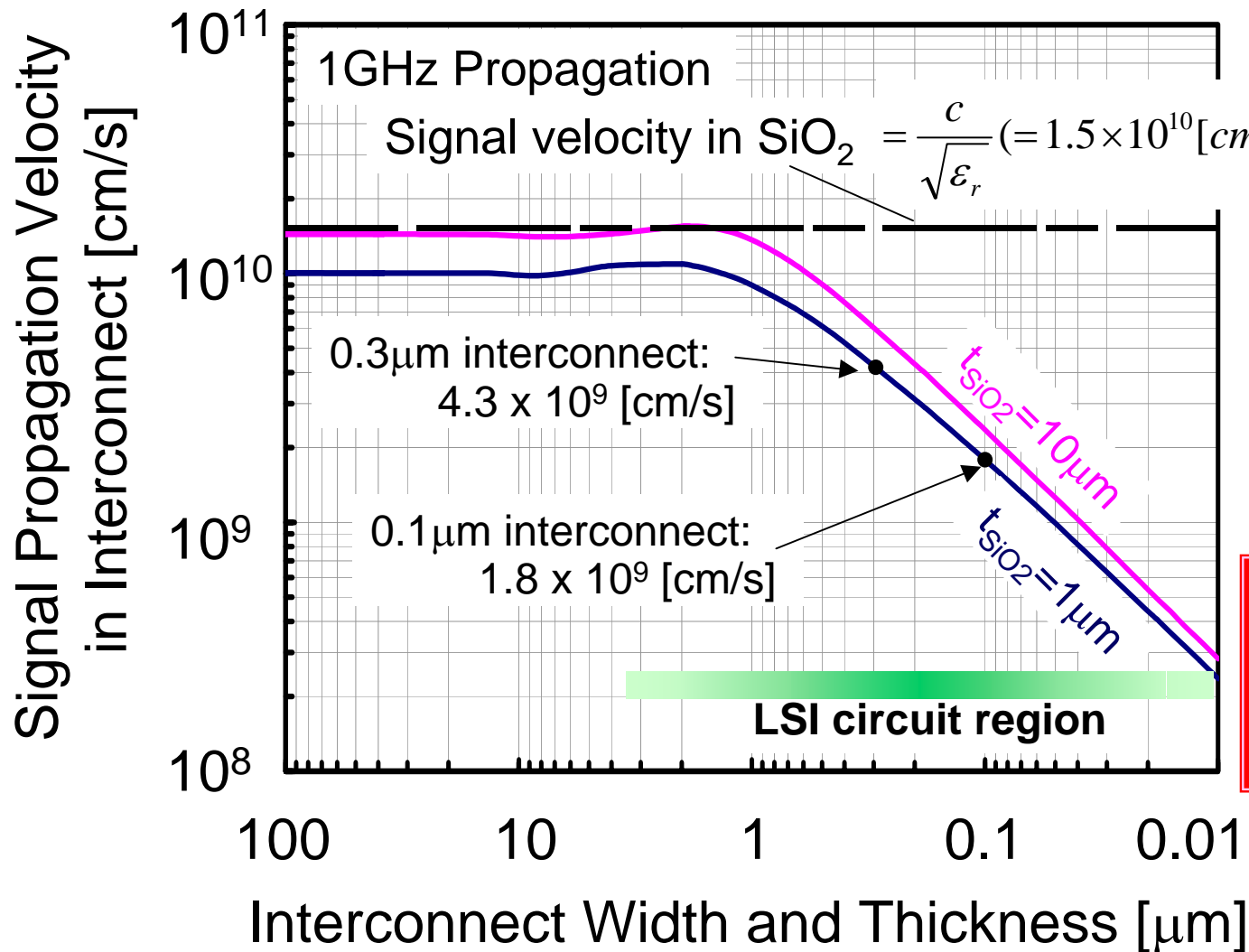


## (110)-oriented MOSFET

2.5 times large current drivability  
 → 1/ 2.5 of Conventional Device  
 Power Consumption

	(100)	(111)	(110)
Current	1.0	1.3	2.5

# Interconnect Performance in LSI circuit



Interconnect in LSI  
 Width & Thickness  
 $<$  Skin Depth



Signal energy is mainly  
 in interconnect metal  
 other than interlayer  
 dielectric in LSI circuit



Signal propagation  
 velocity slows down  
 in LSI circuit region