Low Power CMOS Roadmapping

Dennis Sylvester

University of Michigan
US Design Technology Working Group
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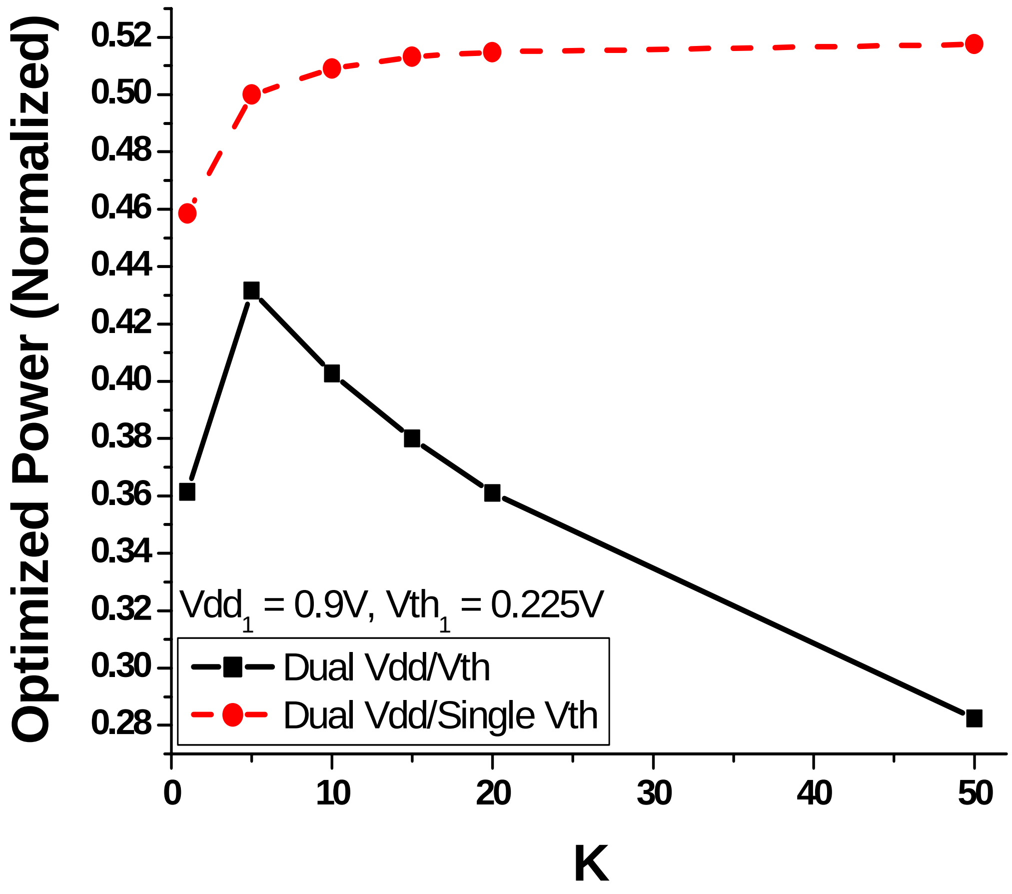
Power = nanometer design driver

- Submicron (0.7-0.35 μm) and deep submicron (0.35~0.13 μm) regimes focused on:
  - Maintaining speed improvements despite lower V_{dd} (move from constant voltage to constant field scaling)
- Nanometer design (≤ 100 nm) will be driven by minimizing power consumption while sustaining throughput and reliability
- Power challenge takes on many forms
  - Low standby power
    - Sleep modes, better devices, circuit approaches, *active mode leakage*
  - Move from being concerned about variability in delay → variability in power
    - Static power sources have exponential dependencies on varying parameters (Vth, Tox, Leff)
  - Design must leverage multi-Vdd/Vth/Tox
    - Tools must comprehend the tradeoffs
    - Libraries need to be either generated on-the-fly or built better originally

Dual Vdd vs. Dual Vdd/Vth

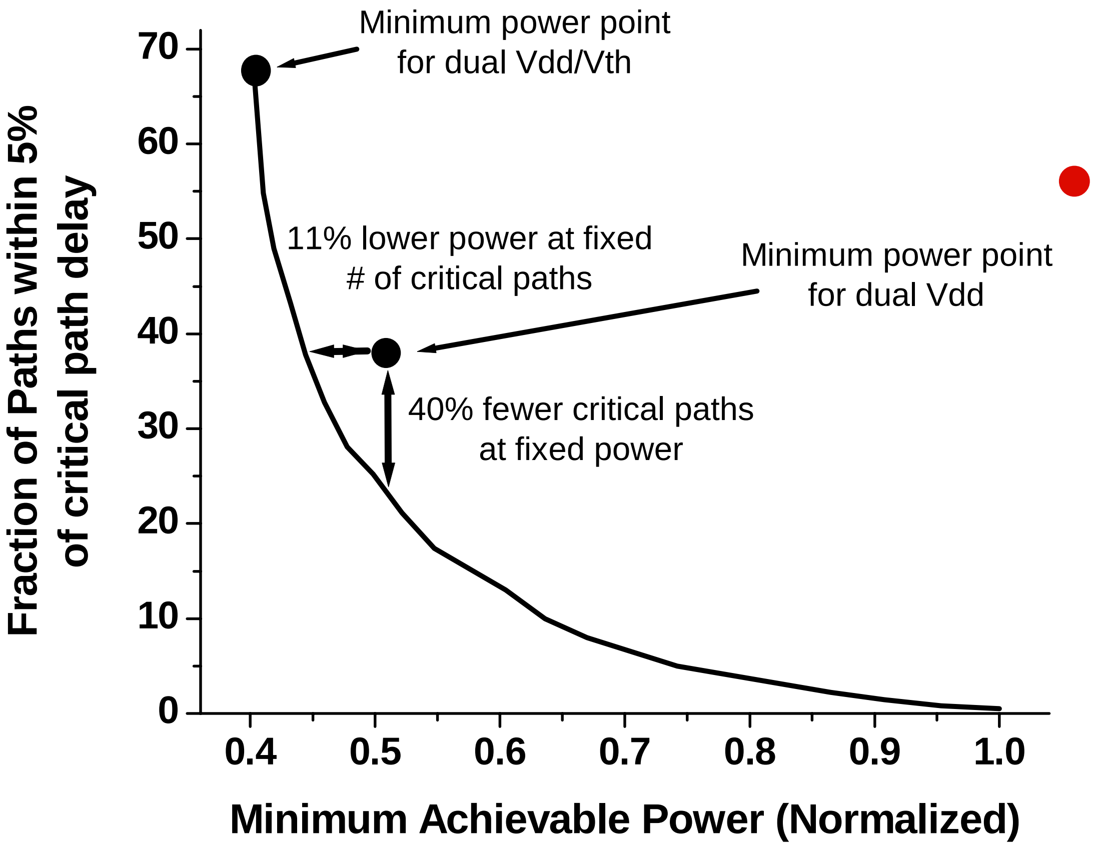


- Define:
  - Dual Vdd as 2 supply voltages with 1 Vth
  - Dual Vdd/Vth has 2 supply and 2 threshold voltages
  - *K* is the ratio of dynamic to static power in initial single Vdd/Vth design
- 2nd Vth and Vdd are found such that total power is minimized ($P_{static} + P_{dynamic}$)
- DIBL is considered

Device scaling impact

- Strained-Si channels
  - Improved mobility, more velocity saturated devices
    - Multi-voltage systems get even better
  - Slowed voltage scaling also leads to more velocity saturation and a better power/delay tradeoff
    - Vdd/Lgate doubles from 130nm to 45nm nodes
- SOI
  - Lowered device (junction) capacitances
    - Sizing is less effective, multi-voltages are comparatively more effective
- Double-gated structures
  - More gate control, better DIBL properties
    - Better Ion/Ioff characteristics
    - Lower Vth for fixed Ioff → can reduce Vdd more aggressively
- Overall: Advanced devices can be leveraged to reduce power; may be more useful than improving speed

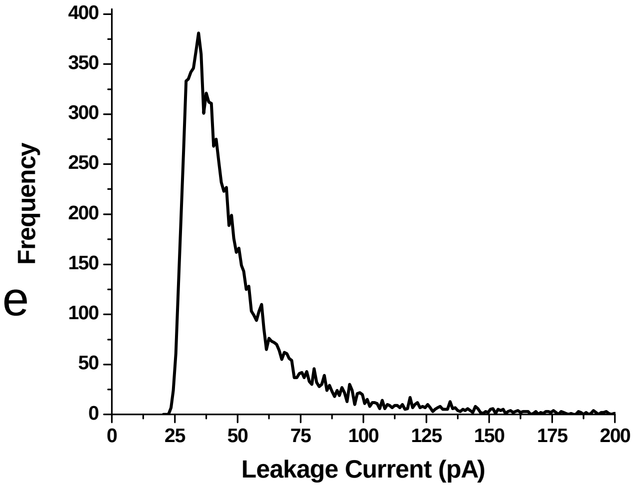
Critical path density



- Critical path density = the fraction of total paths that are critical
- Higher critical path density leads to lower power but more difficult design (variability, timing closure)
  - Strong impact on parametric yield
  - Need for statistical timing analysis

Variability of leakage

- Controlling Vth is increasingly difficult
  - Discrete dopant effects
    - 25nm Leff devices (45nm technology node) show Vth std. deviation of $10/W^{0.5}$ (mV-$\mu m^{0.5}$) [IBM,99]
    - For W_{min} ~ 0.1µm, 3σ Vth uncertainty is 95mV
    - At this technology node, expected Vth values are ~100mV
  - Vth roll-off (with channel length)
- Performance (speed, power) becomes more sensitive to Vth fluctuations in sub-1V technologies
- Corner models for leakage lead to excessive guard banding
  - Since Ioff varies with Vth exponentially, the distribution will be very skewed towards high leakage cases (lognormal)
- Statistical modeling of leakage is desirable
  - Monte Carlo results show that 10% 3σ variation in L_{drawn} gives 22% variation in leakage
    - Variation defined as σ/mean
    - 20% 3σ in L_{drawn} → 79% variability!



Summary

- Power challenge is a broad challenge
  - Variability of static power, critical path density
  - Better libraries needed
  - Static power reduction techniques for active circuitry (not standby)
  - Materials/device structure issue:
    - New devices such as strained-Si, double-gated
    - High-k dielectric to limit static power due to Igate
  - Low power in the face of fault-tolerance/redundancy
- It needs to be addressed in a broad way as well
  - Back off voltages in new device structures to cut power at fixed speed (or increase Vth in standby-limited designs)
  - Statistical timing and power analysis tools
  - Software control (dynamic voltage scaling), architecture
  - Clock network design, especially local clock distribution (latch-level)