International Technology Roadmap for Semiconductors

2000 Update

Test and Test Equipment

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TEST AND TEST EQUIPMENT

SUMMARY

DESIGN DFT REQUIREMENTS

- *Logic BIST*—As digital parts get progressively larger in the future, the external pattern volume (SCAN or other) becomes prohibitive to apply (test time = $$) and still maintain the “high” fault coverage necessary for the desired quality (even with the low-cost ATE). Development of a Logic BIST methodology to get past the tester/DUT bandwidth bottleneck is necessary, and it will be necessary to drive the LBIST coverage to higher and higher fault coverage percentages. The test time problem will be compounded by the addition of non digital content to the DUT.
- *SRAM and DRAM BIST*—Addition of SRAM and DRAM BIST is an economic tradeoff between additional ATE cost of APGs and the cost of implementing these functions on-chip. Also entering into consideration is use in the final application, performance attainable, and tester/DUT bandwidth limitations on pattern application rate.
- *Non contact parametrics*—As pin counts rise higher, the cost of applying parametric tests to the circuitry outside the boundary scan increases. At some point the economics justifies the inclusion of DFT for “non contact parametrics” both from an ATE cost standpoint and a KGD standpoint.
- *Clocking DFT*—Delivering clocks in the high hundreds of MHz with jitter figures in the low tens of picoseconds is costly and somewhat problematic given the performance board constraints and the pin counts and contacting constraints. ATE performance specifications cannot take into account cross-talk and ground bounce induced jitter due to the performance board design, which may be a more significant factor in DUT performance. On-chip clock generation with frequency multiplication is often necessary to prevent the ATE/interface from limiting the chip performance, but a low-jitter clock input from the ATE is still required.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

2000 UPDATE TABLES

*Table NEW DFT-BIST Device Test Requirements—Short Term***

YEAR TECHNOLOGY NODE (nm)	1999 180	2000	2001	2002 130	2003	2004	2005 100	2006	DRIVER
Number of parallel sites		32	32	32	64	64	128	128	Cost
Scan pin count (per site) [1]		128	128	256	256	256	512	512	Logic Density
Scan vector depth (M-Vectors)		128	128	128	256	256	256	256	Logic Density
Scan vector rate (MHz) [2]		50	50	100	100	200	200	200	Test Time
"Full function" pin count (per site) [1]		0-64	0-64	0-64	0-64	0-64	0-64	0-64	Test Time
Functional vector depth (M-Vectors)		2-16	2-16	2-16	2-16	2-16	2-16	2-16	Logic Density
Functional data rate (MHz) [3]		50	100	100	100	200	200	200	Test Time
"Reduced function" pin count (per site) (DC only) [4]		0-2K	0-3K	0-3K	0-3K	0-4K	0-4K	0-5K	I/O Density
High speed clock pins (per site)(differential pairs)		0-4	0-4	0-4	0-4	0-4	0-4	0-4	Clock Domains
High speed clock frequency (MHz) [5]		800	800	800	800	1400	1400	1400	On-chip Clock Rate
Number of power supplies (per site) [6]		8	8	8	8	8	8	8	Logic Density
Power supply voltage / current (per supply)		7V / 8A 4V / 10A	7V / 8A 4V / 10A	7V / 8A 3V / 20A	7V / 8A 3V / 20A	7V / 8A 2V / 40A	7V / 8A 2V / 40A	7V / 8A 2V / 40A	Logic Density / Speed
Support for options (Signature Compression, Memory Algorithmic Pattern Generation, Analog, RF, Serial Communication, High Power and other specialized options)		Yes	Yes	Yes	Yes	Yes	Yes	Yes	SoC / Test Methods

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* **(1999 ITRS)**	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* **(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)**	*1999* *180 nm*	*2000*	*2001* **130 nm**	*2002*	*2003*	*2004* **90nm**	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

Table footnotes

[1] Scan pins and "full function" pins or may be either the same or independent resources, depending on the particular ATE implementation. With scan-only ATE architectures, the scan pins may have a reduced set of waveforms (NRZ and RZ) and may have reduced timing requirements over the conventional "full function" pins.

[2] Edge placement accuracy requirements for scan pins are less than or equal to 10% of the scan period.

[3] Edge placement accuracy requirements for "full function" pins are less than or equal to 0.5% of the functional period.

[4] These pins should support a low frequency (10MHz) and shallow vector depth (4K) functionality.

[5] The accuracy and skew for the high frequency clock pins should be maintained to less than or equal to 8% of the minimum clock period and the jitter should be less than or equal to 1.5% of the minimum clock period.

[6] Both high and low current supplies can be ganged for flexibility.

Other Notes:

This table does not reflect an actual configuration, but rather a consolidation of multiple configurations. Pin counts are per site maximums, however they may not necessarily reflect the per site requirements for configurations with the maximum number of sites. The total number of pins available in any configuration shall be consistent with the current state-of-the-art.

All pins should support basic continuity testing.

This table has undergone radical restructuring since it's last issue. For this reason, the data for 1999 has been removed to avoid confusion.

Table Entry Descriptions

- *Parallel sites*— This requirement refers to the number of discrete devices the platform can be logically segmented to test.
- *Scan pin count*— The number of pins (per site) used for scan data in and out, plus scan control logic. [1]
- *Scan vector depth*— The maximum number of scan vectors that must be supported by each scan pin.
- *Scan vector rate*— The maximum data rate for scan vectors.
- *"Full Function" pin count*—The number of pins (per site) equivalent in function to typical ATE digital pins. [1]
- *Functional vector depth*— The maximum number of vectors that must be supported by each functional pin.
- *Functional data rate*— The maximum data rate for functional vectors.
- *"Reduced Function" pin count*—The number of pins (per site) with typical DC parametric pin functionality.
- *High speed clock pins*— The number of high frequency pins used to drive internal BIST and for AC scan.
- *High speed clock frequency*— The maximum frequency to be supported by the high frequency clock pins. [2]
- *Number of power supplies*— The number of power supply pins (per site)
- *Power supply voltage/current*— The supply voltage and current requirements (per supply)
- *Support for options*— Since it is impossible to anticipate all of the possible ATE resources that might be required for future ASICs and SoCs, a cost effective mechanism for optional resource expansion is required.

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2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

*Flash Technology Requirements***

ITRS Flash Roadmap 2000	*2000*	*2001*	*2002*	*2003*	*2004*	*2005*	*2008*	*2011*	*2014*	*Comments*
Technology	*180 NM*		*130 NM*			*100 NM*	*70 NM*	*50 NM*	*35 NM*	
Device Characteristics										
Density (Megabits): Volume Production	**64**	**64**	**128**	**128**	**256**	**256**	**512**	**2048**	**8192**	
Density (Megabits): Lead Density	**256**	**512**	**512**	**1024**	**1024**	**2048**	**4096**	**16384**	**655356**	
Data width (bits)	**16**	**32**	**32**	**32**	**32**	**32**	**32**	**32**	**32**	
Simultaneously tested devices (wafer test)	**32**	**64**	**64**	**64**	**64**	**64**	**128**	**128**	**256**	
Simultaneously tested devices (package test)	**64**	**64**	**64**	**64**	**64**	**64**	**128**	**128**	**256**	
Power Supplies										
Power supply voltage range	**1.3-5.5**	**0.6-5.5**	**0.6-5.5**	**0.6-5.5**	**0.6-3.3**	**0.6-3.3**	**0.6-3.3**	**0.6-3.3**	**0.6-3.3**	
Power supply accuracy (% of programmed value)	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	
Maximum current (MA)	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**	
Programming power supply voltage range (V)	**1.3-13.0**	**0.6-10.0**	**0.6-10.0**	**0.6-10.0**	**0.6-10.0**	**0.6-10.0**	**0.6-8.0**	**0.6-8.0**	**0.6-8.0**	
Pattern Generator										
Tester Channels	**56**	**64**	**64**	**64**	**64**	**64**	**72**	**72**	**72**	
Vector Depth (millions)	**0.128**	**1**	**1**	**1**	**1**	**1**	**2**	**2**	**2**	
Scan vector depth (millions) (Note 2)	***2***	***2***	***4***	***4***	***4***	***4***	***8***	***8***	***8***	***On chip or multi-chip logic***
APG X, Y, Z Addresses	**16**	**16**	**16**	**16**	**16**	**16**	**16**	**16**	**16**	
Timing										
Max Data Rate (Mhz)	**66**	**80**	**100**	**125**	**133**	**166**	**200**	**250**	**300**	
Accuracy OTA (ns)	**1**	**0.75**	**0.6**	**0.6**	**0.5**	**0.5**	**0.33**	**0.2**	**0.1**	
Cost										
Tester Cost per pin ($) (Note 1)	**1150**	**1000**	**850**	**725**	**610**	**525**	**500**	**450**	**400**	
Reliability										
MTBF (hours)	**2500**	**3000**	**3500**	**4000**	**4500**	**5000**	**6000**	**6500**	**7000**	
MTTR (hours)	**1**	**1**	**1**	**1**	**1**	**1**	**0.5**	**0.5**	**0.5**	
Availability (%)	**98**	**99**	**99**	**99.5**	**99.5**	**99.5**	**99.5**	**99.5**	**99.5**	
Setup Time (hours)	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.2**	**0.2**	**0.2**	**0.2**	

Notes
1. Overall tester cost is: : (per pin cost) x (number of channels) x (number of simultaneously tested).
2. Separate scan-in and scan out.

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