# International Technology Roadmap for Semiconductors

2000 Update

## Metrology

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# METROLOGY

## SUMMARY

### 2000 CD AND OVERLAY METROLOGY

The 1999 potential solutions for CD measurement emphasized CD-SEM as the prevalent method. CD measurements are facing a major roadblock : Meeting the precision requirements for CD control over the next five years. In 2000, the ITWG continued to follow industry based assessment of the depth of focus issues facing CD-SEM. A publication co-authored by F. Mizuno, one of the TWG members, characterized this issue, and indicated that DoF will continue to decrease as resolution is increased to improve precision for future technology generations. DoF has been confirmed as a major roadblock for known CD-SEM technology. Scatterometry has become an accepted method for CD control for specific in-line measurements such as focus – exposure control. Scatterometry is reported to meet precision requirements listed in the near term table for some of 1999 ITRS CD control needs. Scatterometry for contact CD control is not yet commercially available. The ITWG has been asked to add trench sidewall shape and depth (3D) measurement metric (STI, capacitor, trench gate for power device, SOI). A sidewall angle measurement requirement was added in 2000. This is somewhat inadequate because sidewalls are not planar.

Overlay measurements also face some challenges. The metrology community must address Overlay Box-in-Box Target Issues for Phase Shift and Optical Proximity Correction Masks. Overlay structures in kerf (scribe lane) do not represent the intrafield registration adequately.

### FRONT END PROCESSES METROLOGY

Although considerable progress has been made in 2000 toward meeting future requirements for high k materials film thickness measurement and improving precision for oxide gate dielectric film thickness, the challenge remains meeting precision requirements include tool matching. Ultra-shallow junction metrology has an in-line, non-destructive potential solution for the first time, Carrier Illumination.

### NEW DEVICES CHANGE METROLOGY

New devices such dual channel, vertical transistors would significantly change metrology measurements. In these dual channel transistors, CD would be done by film thickness, and gate dielectrics are vertical not horizontal. Thus the metrology community awaits further definition of a device design roadmap.

### INTEGRATED METROLOGY

The ITWG added New Integrated Metrology Requirements for particle detection, end point, and wafer surface temperature.

### INTERCONNECT METROLOGY AND OTHER ISSUES:

Interconnect metal barrier and seed copper metrology is becoming capable of patterned wafer control during CMP. The kerf test structure size needs to be included in future roadmaps, and improved Pattern Recognition is needed.

| 2000 UPDATE | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE (1999 ITRS) | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0) | 1999<br>180 nm | 2000 | 2001<br>130 nm | 2002 | 2003 | 2004<br>90nm | 2005 | 2008<br>[60 NM] | 2011<br>[40 NM] | 2014<br>[30 NM] |

## 2000 UPDATE TABLES

*Table 82a 2000 Metrology Technology Requirements—Near Term***

| 2000 YEAR<br>TECHNOLOGY NODE | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | DRIVER |
|---|---|---|---|---|---|---|---|---|
| DRAM ½ Pitch | 180 | 165 | 150 | 130 | 120 | 110 | 100 | D½ |
| MPU Gate Length | 140 | 120 | 100 | 90 | 80 | 70 | 65 | MPU ASIC |
| New : Final Physical Bottom Gate Length after etch (nm) | 126 | 108 | 90 | 81 | 72 | 63 | 59 | MPU ASIC |
| 2001 YEAR<br>TECHNOLOGY NODE<br>PROPOSED TIMING | 1999<br>180 nm | 2000 | 2001<br>130 nm | 2002 | 2003 | 2004<br>90 nm | 2005 | |
| *Microscopy* | | | | | | | | |
| Inline, nondestructive microscopy resolution (nm) for P/T=0.1<br>P/T >> 0.1 for 1999 and 2000 | 1.3 | 1.1 | 0.9 | 0.8 | 0.7 | 0.6 | 0.6 | MPU Gate |
| Microscopy capable of measurement of patterned wafers having<br>Maximum aspect ratio / diameter (nm) (DRAM contacts) [A] | 6.3<br>200 | 6.7<br>175 | 7.1<br>160 | 7.5<br>140 | 8.0<br>130 | 8.5<br>120 | 9<br>110 | D½ |
| *Materials and Contamination Characterization* | | | | | | | | |
| Real particle detection limit (nm) [B] | 90 | 82 | 75 | 65 | 60 | 55 | 50 | D 1/2 |
| Minimum particle size for compositional analysis (on dense lines) (nm) | 60 | 55 | 50 | 43 | 40 | 37 | 33 | D 1/2 |
| Specification limit of total surface contamination Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, Ni (atoms/cm$^2$) | $\leq 9\times10^9$ | $\leq 7\times10^9$ | $\leq 6\times10^9$ | $\leq 4.4\times10^9$ | $\leq 3.4\times10^9$ | $\leq 2.9\times10^9$ | $\leq 2.5\times10^9$ | MPU Gate |
| Surface detection limits for individual elements Ca, Co, Cu, Cr, Fe, K, Mo, Nm, Na, Ni (atoms/cm$^2$) with signal to noise of 3:1 for each element | $\leq 5.9\times10^8$ | $\leq 5.5\times10^8$ | $\leq 4.2\times10^8$ | $\leq 3.9\times10^8$ | $\leq 2.9\times10^8$ | $\leq 2.4\times10^8$ | $\leq 2.2\times10^8$ | Smallest from MPU or DRAM |

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

*All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.*

| *2000 Update* | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Year of Production<br>Technology Node (1999 ITRS) | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
| Year of Production<br>Technology Node **(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)** | 1999<br>180 nm | 2000 | 2001<br>**130 nm** | 2002 | 2003 | 2004<br>**90nm** | 2005 | 2008<br>**[60 nm]** | 2011<br>**[40 nm]** | 2014<br>**[30 nm]** |

*Table 82b 2000 Metrology Technology Requirements—Long Term***

| Year<br>Technology Node | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm | Driver |
|---|---|---|---|---|
| DRAM ½ Pitch | 70 | 50 | 35 | D½ |
| MPU Gate Length | 45 | 32 | 22 | M Gate |
| **New : Final Physical Bottom Gate Length after Etch** | **41** | **29** | **20** | **M Gate** |
| 2001 Year<br>Technology Node<br>Proposed Timing | 2008<br>**60 nm** | 2011<br>**40 nm** | 2014<br>**30 nm** | |
| *Microscopy* | | | | |
| Inline, nondestructive microscopy resolution (nm) for P/T=0.1 | 0.41 | 0.29 | 0.20 | MPU Gate |
| Maximum aspect ratio / diameter (nm) (DRAM contacts) [A] | 10.5<br>80 | 12<br>60 | 13.5<br>45 | D½ |
| *Materials and Contamination Characterization* | | | | |
| Real particle detection limit (nm) [B] | 35 | 25 | 17 | M Gate |
| Minimum particle size for compositional analysis (on patterned wafers) (nm) | **14** | **9** | **6** | M Gate |
| Specification limit of total surface contamination Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, Ni (atoms/cm$^2$) | $\leq 2.1\times10^9$ | $\leq 1.8\times10^9$ | $\leq 1.7\times10^9$ | M Gate |
| Surface detection limits for individual elements Ca, Co, Cu, Cr, Fe, K, Mo, Nm, Na, Ni (atoms/cm$^2$) with signal to noise of 3:1 for each element | **$\leq 1.9\times10^8$** | **$\leq 1.7\times10^8$** | **$\leq 1.6\times10^8$** | Smallest from MPU or DRAM |

[A} Metal and via aspect ratios are additive for dual-damascene process flow.
[B] This value depends on surface microroughness and layer composition.

Solutions Exist (white) Solutions Being Pursued (yellow) No Known Solutions (red)

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

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| **2000 Update** | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Year of Production<br>Technology Node (1999 ITRS) | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
| Year of Production<br>Technology Node **(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)** | 1999<br>180 nm | 2000 | 2001<br>**130 nm** | 2002 | 2003 | 2004<br>**90nm** | 2005 | 2008<br>**[60 nm]** | 2011<br>**[40 nm]** | 2014<br>**[30 nm]** |

*Table 83a 2000 Lithography Metrology Requirements—Near Term***

| Year<br>Technology Node | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm |
|---|---|---|---|---|---|---|---|
| 2001 Year<br>Technology Node<br>Proposed Timing | 1999<br>180 nm | 2000 | 2001<br>**130 nm** | 2002 | 2003 | 2004<br>**90 nm** | 2005 |
| Wafer gate CD control | 13 | 10.8 | 9.0 | 8.1 | 7.2 | 6.3 | 5.9 |
| Wafer dense line CD control | 18 | 16.5 | 15 | 13 | 12 | 11 | 10 |
| Wafer contact CD control | 20 | 18.5 | 17 | 15 | 14.5 | 14 | 13 |
| Wafer CD metrology tool precision*<br>P/T=.2 for isolated lines** | 2.6 | 2.2 | 1.8 | 1.6 | 1.4 | 1.3 | 1.2 |
| Wafer CD metrology tool precision*<br>P/T=.2 for dense lines** | 3.6 | 3.3 | 3.0 | 2.6 | 2.4 | 2.2 | 2.0 |
| Wafer CD metrology tool precision*<br>P/T=.2 for contacts** | 4.0 | 3.7 | 3.4 | 3.0 | 2.9 | 2.6 | 2.3 |
| Wafer sidewall angle accuracy (in degrees) *Depth of Focus ~ 1 µm* | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| Maximum CD measurement bias (%) | 10 | 10 | 10 | 10 | 10 | 10 | 10 |
| Mask CD control isolated lines | 16 | 14 | 12 | 10 | 9 | 8 | 7 |
| Mask CD control dense lines | 24 | 21 | 17 | 13 | 12 | 11 | 10 |
| Mask contact area control<br>Normalized to ρ of Area | 24 | 21 | 17 | 14 | 13 | 12 | 11 |
| Mask CD metrology tool precision*<br>P/T=.2 for isolated lines** | 3.2 | 2.8 | 2.4 | 2 | 1.8 | 1.6 | 1.4 |
| Mask CD metrology tool precision* P/T=.2 for dense lines** | 4.8 | 4.2 | 3.4 | 2.6 | 2.4 | 2.2 | 2 |
| Mask area metrology tool precision for contact normalized to ρ of area–ρ of target for P/T=.2 | 4.8 | 4.2 | 3.4 | 2.8 | 2.6 | 2.4 | 2.2 |
| Wafer overlay control (nm) | 65 | 58 | 52 | 45 | 42 | 38 | 35 |
| Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1 | 6.5 | 5.8 | 5.2 | 4.5 | 4.2 | 3.8 | 3.5 |
| Final mask image placement | 39 | 35 | 31 | 27 | 25 | 23 | 21 |
| Mask image placement<br>Metrology precision P/T=.1 | 3.9 | 3.5 | 3.1 | 2.7 | 2.5 | 2.3 | 2.1 |
| Mask phase (in degrees) | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Phase metrology precision P/T=.2 (in degrees) | .4 | .4 | .4 | .4 | .4 | .4 | .4 |
| Variation in attenuated mask film transmission % of deviation from nominal (%) | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Transmission metrology precision % of nominal attenuated psm transmission P/T=.2 (%) | .8 | .8 | .8 | .8 | .8 | .8 | .8 |

* *All precision values are 3 sigma in nm and include metrology tool matching.*
** *Measurement tool performance needs to be independent of line shape, line materials, and density of lines.*

*Solutions Exist* *Solutions Being Pursued* *No Known Solutions*

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| 2000 UPDATE | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE (1999 ITRS) | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0) | 1999<br>180 nm | 2000 | 2001<br>**130 nm** | 2002 | 2003 | 2004<br>**90nm** | 2005 | 2008<br>[60 NM] | 2011<br>[40 NM] | 2014<br>[30 NM] |

*Table 83b 2000 Lithography Metrology Requirements—Long Term***

| YEAR<br>TECHNOLOGY NODE | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
|---|---|---|---|
| 2001 YEAR<br>TECHNOLOGY NODE<br>PROPOSED TIMING | 2008<br>**60 nm** | 2011<br>**40 nm** | 2014<br>**30 nm** |
| Wafer gate CD control | 4.0 | 3.0 | 2.0 |
| Wafer dense line CD control | 7.0 | 5.0 | 3.5 |
| Wafer contact CD control | 8.0 | 5.5 | 4.0 |
| Wafer CD metrology tool precision*<br>P/T=.2 for isolated lines** | 0.8 | 0.6 | 0.4 |
| Wafer CD metrology tool precision*<br>P/T=.2 for dense lines** | 1.4 | 1.0 | 0.7 |
| Wafer CD metrology tool precision*<br>P/T=.2 for contacts** | 1.6 | 1.1 | 0.8 |
| Wafer sidewall angle accuracy (in degrees)<br>*Depth of Focus ~ 1 µm* | 0.5 | 0.5 | 0.5 |
| Maximum CD measurement bias (%) | 10 | 10 | 10 |
| Mask CD control isolated lines | 7 | 5 | 3.3 |
| Mask CD control dense lines | 11 | 8 | 5.6 |
| Mask contact area control<br>Normalized to ρ of area | 12 | 9 | 6.4 |
| Mask CD metrology tool precision*<br>P/T=.2 for isolated lines** | 1.4 | 1.0 | 0.7 |
| Mask CD metrology tool precision*<br>P/T=.2 for dense lines** | 2.2 | 1.6 | 1.1 |
| Mask area metrology tool precision for contact normalized to ρ of area–ρ of target for P/T=.2 | 1.6 | 1.8 | 1.3 |
| Wafer overlay control (nm) | 25 | 20 | 15 |
| Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1 | 2.5 | 2.0 | 1.5 |
| Final mask image placement | 15 | 12 | 9 |
| Mask image placement<br>metrology precision P/T=.1 | 1.5 | 1.2 | 0.9 |
| Mask phase (in degrees) | 1 | NA | NA |
| Phase metrology precision P/T=.2 (in degrees) | 0.2 | NA | NA |
| Variation in attenuated mask film transmission % of deviation from nominal (%) | 4 | NA | NA |
| Transmission metrology precision % of nominal attenuated PSM transmission P/T=.2 (%) | 0.8 | NA | NA |

* *All precision values are 3 sigma in nm and include metrology tool matching.*
** *Measurement tool performance needs to be independent of line shape, line materials, and density of lines*

*Solutions Exist* (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

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| *2000 Update* | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| *Year of Production*<br>*Technology Node* ***(1999 ITRS)*** | *1999*<br>*180 nm* | *2000* | *2001* | *2002*<br>*130 nm* | *2003* | *2004* | *2005*<br>*100 nm* | *2008*<br>*70 nm* | *2011*<br>*50 nm* | *2014*<br>*35 nm* |
| *Year of Production*<br>*Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)*** | *1999*<br>*180 nm* | *2000* | *2001*<br>***130 nm*** | *2002* | *2003* | *2004*<br>***90nm*** | *2005* | 2008<br>**[60 nm]** | 2011<br>**[40 nm]** | 2014<br>**[30 nm]** |

*Table 84a 2000 Front End Processes Metrology Technology Requirements—Near Term***

| Year<br>Technology Node | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | Driver |
|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch* | 180 | 165 | 150 | 130 | 120 | 110 | 100 | D½ |
| *MPU Gate Length* | 140 | 120 | 100 | 85 | 80 | 70 | 65 | M Gate |
| *MPU Gate Length* | 140 | 120 | 100 | ***90*** | 80 | 70 | 65 | MPU gate |
| **New : Final Physical Bottom Gate Length after etch (nm)** | **126** | **120** | **100** | **90** | **80** | **70** | **65** | **MPU ASIC** |
| *2001 Year*<br>*Technology Node*<br>*Proposed Timing* | *1999*<br>*180 nm* | *2000* | *2001*<br>***130 nm*** | *2002* | *2003* | *2004*<br>***90 nm*** | 2005 | |
| Oxygen range ( ASTM "79) in heavily doped substrates; measurement precision ± 0.5 ppma [A] | ***19***–**31** | **18–31** | **18–31** | **18–31** | **18–31** | **18–31** | **18–31** | |
| Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm³) | **$1 \times 10^{10}$** | **$< 1 \times 10^{10}$** | **$< 1 \times 10^{10}$** | **$< 1 \times 10^{10}$** | **$< 1 \times 10^{10}$** | **$< 1 \times 10^{10}$** | **$< 1 \times 10^{10}$** | |
| Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm³) | **$1 \times 10^{9}$** | **$< 1 \times 10^{9}$** | **$< 1 \times 10^{9}$** | **$< 1 \times 10^{9}$** | **$< 1 \times 10^{9}$** | **$< 1 \times 10^{9}$** | **$< 1 \times 10^{9}$** | |
| Logic dielectric equivalent thickness (nm) ± 3σ process range | **1.9–2.5 ± 4%** | **1.9–2.5 ± 4%** | **1.5–1.9 ± 4%** | **1.5–1.9 ± 4%** | **1.5–1.9 ± 4%** | **1.2–1.5 ± 4%** | **1.0–1.5 ± 4%** | MPU Gate |
| Logic dielectric measurement precision 3σ (nm) [B] | **0.0075** | **0.0075** | **0.006** | **0.006** | **0.006** | **0.005** | **0.004** | M Gate |
| DRAM capacitor structure dielectric material process control requirements<br><br>(Dielectric constant)<br>Equivalent oxide thickness (nm) | **Cyl. MIS $Ta_2O_5$ (22) 3.0** | **Cyl. MIS $Ta_2O_5$ (22) 3.0** | **Cyl. MIS $Ta_2O_5$ (22) 3.0** | **Pedestal MIM $Ta_2O_5$ (50) 0.95** | **Pedestal MIM $Ta_2O_5$ (50) 0.95** | **Pedestal MIM $Ta_2O_5$ (50) 0.95** | **Pedestal MIM BST (250) 0.45** | D½ |
| DRAM capacitor dielectric physical thickness (nm) ± 3 σ process range | **11.5 ±4%** | **11.5 ±4%** | **11.5 ±4%** | **12.2 ±4%** | **12.2 ±4%** | **12.2 ±4%** | **28.7 ±4%** | D½ |
| DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) [C] | **0.046** | **0.046** | **0.046** | **0.049** | **0.049** | **0.049** | **0.11** | D½ |
| 2 and 3D dopant profile spatial resolution (nm) | **3** | **3** | **3** | **2** | **2** | **2** | **1.5** | |
| At-line dopant concentration precision (across concentration range) [D] | **5%** | **5%** | **5%** | **4%** | **4%** | **4%** | **3%** | |

*Solutions Exist* (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

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*All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.*

| 2000 UPDATE | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE (1999 ITRS) | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)** | 1999<br>180 nm | 2000 | 2001<br>**130 nm** | 2002 | 2003 | 2004<br>**90nm** | 2005 | 2008<br>**[60 NM]** | 2011<br>**[40 NM]** | 2014<br>**[30 NM]** |

*Table 84b 2000 Front End Processes Metrology Technology Requirements—Long Term***

| YEAR<br>TECHNOLOGY NODE | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm | Driver |
|---|---|---|---|---|
| 2001 YEAR<br>TECHNOLOGY NODE<br>PROPOSED TIMING | 2008<br>**60 nm** | 2011<br>**40 nm** | 2014<br>**30 nm** | |
| DRAM 1/2 Pitch | 70 | 50 | 35 | |
| **New : Final Physical Bottom Gate Length after Etch** | **41** | **29** | **20** | MPU Gate |
| Oxygen range ( ASTM "79) in heavily doped substrates; measurement precision ± 0.5 ppma [A] | 18 – 31 | 18–31 | 18–31 | |
| Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/$cm^3$) | $< 1 \times 10^{10}$ | $< 1 \times 10^{10}$ | $< 1 \times 10^{10}$ | |
| Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/$cm^3$) | $< 1 \times 10^{9}$ | $< 1 \times 10^{9}$ | $< 1 \times 10^{9}$ | |
| Logic dielectric equivalent thickness (nm) ± 3σ process range | 0.8–1.2<br>± 4% | 0.6–0.8<br>± 4% | 0.5–0.6<br>± 4% | MPU |
| Logic dielectric measurement precision 3σ (nm) [B] | 0.0032 | 0.0024 | 0.002 | MPU |
| DRAM capacitor structure dielectric material process control requirements<br><br>(Dielectric constant)<br>Equivalent oxide thickness (nm) | Pedestal<br>MIM<br>epi-BST<br>(700)<br>0.15 | Pedestal<br>MIM<br>???<br>(1500)<br>0.060 | Pedestal<br>MIM<br>???<br>(1500)<br>0.043 | D ½ |
| DRAM capacitor dielectric physical thickness (nm) ±3σ process range [C] | 27.2<br>± 4% | 23.0<br>4% | 16.4<br>4% | D ½ |
| DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) | 0.11 | 0.092 | 0.066 | D ½ |
| 2 and 3D dopant profile spatial resolution (nm) | 1 | 0.8–0.6 | 0.8–0.6 | |
| At-line dopant profile concentration precision (across concentration range) [D] | 2% | 2% | 2% | |

*Solutions Exist* (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

*Notes for Table 84 for Front End Processes Metrology Requirements*

*[A] IOC '88 value obtained by multiplying ASTM value by 0.65.*

*[B] Precision calculated from P/T=0.1=6×precision/process range. The measurement requirements specify the equivalent thickness for a silicon dioxide dielectric film. It is expected that oxynitirides and stacked nitride/silicon dioxide layers will replace silicon dioxide for the 130 and 100 nm logic generations and that high dielectric constant materials such as $Ta_2O_5$ will be used at and after the 70 nm logic node and possibly at the 100 nm node. The physical thickness of the high dielectric constant layer can be calculated by multiplying the ratio of the dielectric constants ($\mathcal{E}_{high\ \kappa} / \mathcal{E}_{ox}$) by the effective oxide thickness. For example, a 6.4 nm thick $Ta_2O_5$ (κ= ~25) layer has a 1 nm equivalent oxide (κ=3.9) thickness. The listed precision is based on equivalent oxide thickness and must be multiplied by the ratio of the dielectric constant to obtain precision for the dielectric of interest. The total capacitance of the dielectric stack also includes that of the dielectric layer plus the interfacial layer, quantum state effects at the channel interface, and that*

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*All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.*

| *2000 UPDATE* | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE **(1999 ITRS)** | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)** | 1999<br>180 nm | 2000 | 2001<br>**130 nm** | 2002 | 2003 | 2004<br>**90nm** | 2005 | 2008<br>**[60 NM]** | 2011<br>**[40 NM]** | 2014<br>**[30 NM]** |

*associated with depletion of charge in the poly silicon gate electrode. Thus, the challenge to gate dielectric thickness measurement includes metrology for the interfacial layer.*

[C] *In the case of MIS structure, physical thickness, $t_{diel}$ , is calculated using the equation of $t_{diel}=(t_{eq.ox}-1\ nm)_{diel}\,\varepsilon_{high\ \kappa}/3.9$ in which oxide film formed at the interface of poly-silicon and dielectric material in annealing is taken into account. In the case of MIM structure, $t_{diel}$ is calculated using the equation of $t_{diel}= t_{eq.ox}\,\varepsilon_{high\ \kappa}/3.9$ . Here $t_{eq.ox}$ is equivalent oxide thickness, and $t_{diel}$ is dielectric constant of the dielectric material.*

[D] *High precision measurements with low systematic error are required.*

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*All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.*

| 2000 UPDATE | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE (1999 ITRS) | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)** | 1999<br>180 nm | 2000 | 2001<br>**130 nm** | 2002 | 2003 | 2004<br>**90nm** | 2005 | 2008<br>**[60 NM]** | 2011<br>**[40 NM]** | 2014<br>**[30 NM]** |

*Table 85a 2000 Interconnect Metrology Technology Requirements—Near Term***

| YEAR<br>TECHNOLOGY NODE | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 20005<br>100 nm | DRIVER |
|---|---|---|---|---|---|---|---|---|
| DRAM 1/2 Pitch | 180 | 165 | 150 | 130 | 120 | 110 | 100 | |
| MPU Gate Length | 140 | 120 | 100 | 85 | 80 | 70 | 65 | |
| MPU Gate Length | 140 | 120 | 100 | **90** | 80 | 70 | 65 | MPU gate |
| **New : Final Physical Bottom Gate Length after etch (nm)** | **126** | **120** | **100** | **90** | **80** | **70** | **65** | **MPU ASIC** |
| 2001 YEAR<br>TECHNOLOGY NODE<br>PROPOSED TIMING | 1999<br>180 nm | 2000 | 2001<br>**130 nm** | 2002 | 2003 | 2004<br>90 nm | 2005 | |
| Planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm)<br>Measurement precision (nm) | **25 × 32<br>250<br>± 25** | **250** | **250** | **25 × 36<br>200<br>±20** | **200** | **200** | **25 × 40<br>175<br>±17** | MPU |
| Measurement of deposited barrier layer at thickness (nm) / process range (± 3σ ) precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers [A] | **17/10%<br><0.06** | **16/10%<br>0.05** | **14/10%<br><0.05** | **13/10%<br>0.04** | **12/10%<br>0.04** | **11/10%<br><0.04** | **10/10%<br>0.03** | **MPU** |
| Measure interlevel metal insulator effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× local clock frequency (GHz) [B] | **2.9<br>1.25** | **2.9** | **2.7** | **2.7<br>2.1** | **2.0** | **2.0** | **1.3<br>3.5** | **MPU** |

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

*All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.*

| ***2000 Update*** | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| *Year of Production*<br>*Technology Node* ***(1999 ITRS)*** | *1999*<br>*180 nm* | *2000* | *2001* | *2002*<br>*130 nm* | *2003* | *2004* | *2005*<br>*100 nm* | *2008*<br>*70 nm* | *2011*<br>*50 nm* | *2014*<br>*35 nm* |
| *Year of Production*<br>*Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)*** | *1999*<br>*180 nm* | *2000* | *2001*<br>***130 nm*** | *2002* | *2003* | *2004*<br>***90nm*** | *2005* | 2008<br>**[60 nm]** | 2011<br>**[40 nm]** | 2014<br>**[30 nm]** |

*Table 85b 2000 Interconnect Metrology Technology Requirements—Long Term***

| *Year*<br>*Technology Node* | *2008*<br>*70 nm* | *2011*<br>*50 nm* | *2014*<br>*35 nm* | *Driver* |
|---|---|---|---|---|
| *2001 Year*<br>*Technology Node*<br>*Proposed Timing* | *2008*<br>***60 nm*** | *2011*<br>***40 nm*** | *2014*<br>*30 nm* | |
| Planarity requirements: lithography field (mm × mm)/ planarity for minimum interconnect CD (nm) / measurement precision | **25 × 44**<br>**175**<br>**±17** | **25 × 52**<br>**175**<br>**±17** | **175**<br>**±17** | *MPU* |
| ***Measurement of deposited barrier layer At Thickness (nm)/process range (± 3σ) Precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers [A]*** | **7/10%**<br>**< 0.024** | **5/10%**<br>**<0.017** | **4/10%**<br>**< 0.013** | *MPU* |
| Measure interlevel metal insulator effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× clock frequency (GHz) [B] | **2.5 – 3.0**<br>**6** | **2.0 – 2.5**<br>**10** | **2.0 – 2.3**<br>**17** | *MPU* |

*Notes for Table 85 for Interconnect Metrology Requirements*

*[A} Roadmap predicts barrier for 35 nm technology node will be formed by reactive processes in metal or dielectric or both instead of by deposition.*

*[B] Minimum effective dielectric constant is listed. Due to divergence of DRAM and logic requirements, minimum listed number is associated with logic requirements. The development of a measurement technique for low κ dielectric constant and anisotropy is nearly complete up to 40 GHz. Technology transfer to industry will take place from 1999 to 2000.*

*Solutions Exist* (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

*All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.*

| 2000 Update | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Year of Production<br>Technology Node (1999 ITRS) | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
| Year of Production<br>Technology Node (Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0) | 1999<br>180 nm | 2000 | 2001<br>130 nm | 2002 | 2003 | 2004<br>90nm | 2005 | 2008<br>[60 nm] | 2011<br>[40 nm] | 2014<br>[30 nm] |

## New Metrology Tables

*In-situ /on-line Particle Detection for Pure Water and Liquid Chemicals***

| First Year of Shipment<br>Technology Node | 1999<br>180 nm | 2002<br>130 nm | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
|---|---|---|---|---|---|---|
| Critical particle size (nm) | 90 | 65 | 45 | 35 | 25 | 17 |
| Particle detection limit (nm) | 90 | 65 | 45 | 35 | 25 | 17 |

*In-situ Film Thickness Measurement for Stacked Metal Layers (CMP End Point Monitor)***

| First Year of Shipment<br>Technology Node | 1999<br>180 nm | 2002<br>130 nm | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
|---|---|---|---|---|---|---|
| Metal layer<br>Materials<br>Thickness (nm)<br>Thickness control (nm, 3σ) | Cu barrier<br>metal film<br>350<br>35 | Cu barrier<br>metal film<br>274<br>27 | Cu barrier<br>metal film<br>225<br>23 | single Cu<br><br>176<br>18 | single Cu<br><br>137<br>14 | single Cu<br><br>109<br>11 |
| Measurement precision of film thickness (nm, 3σ, P/T=0.1) | 3.5 | 2.7 | 2.3 | 1.8 | 1.4 | 1.1 |
| Response time for film thickness measurement [1)] (s) | 0.035 | 0.027 | 0.023 | 0.018 | 0.014 | 0.011 |
| Linewidth of measured metal wire ( nm) [2] | 180 | 130 | 100 | 70 | 50 | 35 |

1) The response time requirements have been determined to be 1/10 of each process time required at a Cu CMP speed of 10 nm/s.

2) Film thickness measurements on metal wires are ideal, but if it is impossible the use of measurement patterns would be possible as the second choice. The measurement patterns should be located in the scribe area and have the minimum size of 60 m x 60 m.

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*All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.*

| 2000 UPDATE | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE (1999 ITRS) | 1999<br>180 nm | 2000 | 2001 | 2002<br>130 nm | 2003 | 2004 | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
| YEAR OF PRODUCTION<br>TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0) | 1999<br>180 nm | 2000 | 2001<br>130 nm | 2002 | 2003 | 2004<br>90nm | 2005 | 2008<br>[60 NM] | 2011<br>[40 NM] | 2014<br>[30 NM] |

*In-situ Wafer Surface Temperature Measurement for RTP and Plasma Process***

| First Year of Shipment<br>Technology Node | 1999<br>180 nm | 2002<br>130 nm | 2005<br>100 nm | 2008<br>70 nm | 2011<br>50 nm | 2014<br>35 nm |
|---|---|---|---|---|---|---|
| RTP for carrier activation<br>Process temperature (°C)<br>Temperature control (°C, 3σ) | 600-1100<br>1 | 600-1000<br>1 | 600-1000<br>1 | 600-900<br>1 | 600-900<br>1 | 600-900<br>1 |
| Ramp speed of process temperature (°C /s) | 150 | 200 | 250 | >350 | >350 | >500 |
| Measurement precision of wafer surface temperature (°C, 3σ) | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 |
| Spatial resolution for temperature measurement (mm) | 1 | 1 | 1 | 1 | 1 | 1 |
| Time resolution for temperature measurement ( ms) [1] | 0.67 | 0.5 | 0.4 | <0.29 | <0.29 | <0.2 |
| Plasma process<br>Process temperature (°C)<br>Temperature control (°C, 3σ) | 30-500<br>5 | 30-500<br>5 | 30-500<br>5 | 30-500<br>5 | 30-500<br>5 | 30-500<br>5 |
| Ramp speed of process temperature (°C /s) | 20 | 20 | 20 | 20 | 20 | 20 |
| Measurement precision of wafer surface temperature (°C, 3σ) | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 |
| Spatial resolution for temperature measurement (mm) | 1 | 1 | 1 | 1 | 1 | 1 |
| Time resolution for temperature measurement (ms) [1] | 5 | 5 | 5 | 5 | 5 | 5 |

1) The time resolution requirements have been determined to be P/T=0.1 for each ramp time (s/°C).

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

*All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.*