International Technology Roadmap for Semiconductors

2000 Update

Front End Processes

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FRONT END PROCESSES

SUMMARY

In the year since publication of the 1999 ITRS document, it has become clear that some of the forecast assumptions used to guide the FEP chapter and tables were too conservative and are consequently in need of adjustment. Specifically, it has been observed that:

1. Technology node timing, as measured by the DRAM and MPU/ASIC half pitch scaling is proceeding faster than originally forecasted.
2. Transistor scaling, as measured by the MPU Gate length is also proceeding faster than originally forecasted
3. The time gap between MPU and ASIC Gate lengths had been substantially eliminated

In addition, the FEP TWG has received comments from many DRAM manufacturers suggesting that memory storage node scaling, as defined by the 1999 DRAM cell "a" factor is too aggressive.

Finally, in this past year, new insights have been gained from chip size/functionality forecasts and concomitant productivity analyses, suggesting that the need for the wafer sizes beyond 300mm (450mm?) might occur earlier than forecasted in the 1999 ITRS.

The international technology working groups that have been analyzing these issues, and have reached consensus on DRAM storage node scaling, that has resulted in substantial year 2000 updates to tables 35 and 36 of the FEP chapter.

However, consensus has not yet been reached on technology node timing issues related to DRAM and MPU ½ pitch, as well as MPU/ASIC gate length scaling, nor has consensus be achieved on wafer size forecasts. These forecasts remain in the proposal stage, with the objective of achieving consensus by year end. As a consequence the remaining tables of the FEP chapter have not been changed except to reflect current reality, remove errors, or introduce new values that result from enhancements to yield/defect and/or transistor scaling models. However, the new proposed technology node parameter values have been posted to the tables, with explanatory footnotes to keep the reader aware that the tables have not been updated with these new, proposed, parameters. It is left to the table reader approximate the impact of this node acceleration on the table values. It is expected that consensus and table updating will comprise the major year 2001 initiatives leading to the publication of the 2001 ITRS.

A major year 2001 issue for the international FEP technology working groups is the faster than forecasted reduction in MOSFET gate length. This implies the need for CMOS integration of high-k gate dielectrics, and dual metal gates, <u>earlier than year 2005</u>, that was originally forecasted in the 1999 ITRS document. While developmental progress in this area has been significant, it becomes increasingly probable that chip production with high-k gate stacks will be very difficult to achieve in the 2005 time frame, and therefore appears unlikely in the more accelerated time frames suggested by the new proposed gate length scaling forecasts. Consequently, a major 2001 task is the analysis of this trend, and the identification of design, device, and material alternatives imposed by the difficulties of accelerated high-k/dual metal gate CMOS integration.

2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

2000 Update Tables

*Table 32a Starting Materials Technology Requirements—Near Term***

Year of First Product Shipment *Technology Node*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*Driver*
Proposed Year of First Product Shipment,, ***Technology Node (A)***	*1999* *180 nm*	*2000*	***2001*** ***130nm***	*2002*	***2003*** ***100 nm***	*2004*	*2005*	*Driver*
DRAM 1/2 Pitch (nm)	**180**	**165**	**150**	**130**	**120**	**110**	**100**	**D ½**
New DRAM 1/2 Pitch (nm) (A)	**180**	**150**	***130***	***115***	***100***	***90***	***80***	***D ½***
MPU Gate Length (nm)	**140**	**120**	**100**	**85**	**80**	**70**	**65**	**M**
New MPU/ASIC Gate Length (In Resist) (nm) (A)	***140***	***120***	***100***	***90***	***80***	***70***	***65***	***M***
General Characteristics * (B,C)								
Wafer diameter (mm) **	**200**	**300 *****	**300**	**300**	**300**	**300**	**300**	**D ½, M**
Edge exclusion (mm) ****	**3**	**3**	**3**	**3**	**1**	**1**	**1**	**D ½, M**
Front surface particle size (nm), latex sphere equivalent (D)	≥ 90	***≥ 90***	***≥ 90***	***≥ 90***	≥ 60	≥ 55	≥ 50	***D ½, M***
Particles (cm^{-2}) (E,F)	≤ 0.13	≤ 0.12	≤ 0.12	≤ 0.14	≤ 0.13	≤ 0.12	≤ 0.10	***D ½, M***
Particles (#/wf)	≤ 38	***≤81***	***≤ 78***	***≤93***	≤ 89	≤ 84	≤ 72	***D ½, M***
Critical surface metals (at/cm^{2}) (G)	≤ 1.8E+10	≤ 1.4E+10	≤ 1.2E+10	≤ 8.8E+9	≤ 6.8E+9	≤ 5.8E+9	≤ 4.9E+9	**D ½, M**
Site flatness (nm) (H)	≤ 180	≤ 165	≤ 150	≤ 130	≤ 120	≤ 110	≤ 100	***D ½, M***
Oxygen (center point value ± 2.0 ppma) (ASTM '79) (I)	**19–31**	**18–31**	**18–31**	**18–31**	**18–31**	**18-31**	**18-31**	**D ½, M**
Polished Wafer *								
Total Allowable Front Surface Light Scattering Defect Density is The Sum of Crystal Originated Pits (COPs) and Particles (see General Characteristics)								
Front surface COPs size (nm), latex sphere equivalent (D)	≥ 90	***≥ 90***	***≥ 90***	***≥ 90***	≥ 60	≥ 55	≥ 50	***D ½, M***
COPs (cm^{-2}) (J)	≤ 0.13	≤ 0.12	≤ 0.12	≤ 0.14	≤ 0.13	≤ 0.12	≤ 0.10	***D ½, M***
COPs (#/wf)	≤ 38	***≤ 81***	***≤ 78***	***≤93***	≤ 89	≤ 84	≤ 72	***D ½, M***
Total bulk Fe (at/cm^{3}) (K)	**≤ 1 x 10^{10}**	**< 1 x 10^{10}**	**< 1 x 10^{10}**	**< 1 x 10^{10}**	**< 1 x 10^{10}**	**< 1 x 10^{10}**	**< 1 x 10^{10}**	**D ½, M**
Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) (L)	≤ 4.4	≤ 3.9	≤ 3.4	≤ 2.8	≤ 2.5	≤ 2.2	≤ 1.9	**D ½**
Oxidation stacking faults (OSF) (MPU) (cm^{-2}) (L)	≤ 3.1	≤ 2.5	≤ 1.9	≤ 1.5	≤ 1.4	≤ 1.1	≤ 1.0	**M**
Epitaxial Wafer *								
Total Allowable Front Surface Defect Density is The Sum of Epitaxial Large Area Defects, Epitaxial Stacking Faults and Particles (see General Characteristics) (M,N)								
Layer large area defects (DRAM) (cm^{-2}) (O)	≤ 0.008	≤ 0.007	≤ 0.007	≤ 0.007	≤ 0.006	≤ 0.006	≤ 0.006	**D ½**
Layer large area defects (MPU) (cm^{-2}) (O)	≤ 0.006	≤ 0.006	≤ 0.006	≤ 0.006	≤ 0.006	≤ 0.006	≤ 0.006	**M**
Layer stacking faults (DRAM) (cm^{-2}) (P)	≤ 0.015	≤ 0.015	≤ 0.014	≤ 0.013	≤ 0.013	≤ 0.012	≤ 0.012	**D ½**
Layer stacking faults (MPU) (cm^{-2}) (P)	≤ 0.012	≤ 0.012	≤ 0.012	≤ 0.012	≤ 0.012	≤ 0.012	≤ 0.012	**M**

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production Technology Node (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Year of Production Technology Node (Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]

*Table 32a Starting Materials Technology Requirements—Near Term (continued)***

Year of First Product Shipment Technology Node	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
Proposed Year of First Product Shipment, Technology Node (A)	1999 180 nm	2000	2001 130nm	2002	2003 100 nm	2004	2005	
DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	D ½
New DRAM ½ Pitch (nm) (A)	180	150	130	115	100	90	80	D ½
MPU Gate Length (nm)	140	120	100	85	80	70	65	M
New MPU/ASIC Gate Length (In Resist) (nm) (A)	140	120	100	90	80	70	65	M
*Silicon-On-Insulator Wafer**								
Wafer diameter (mm)	200	200	200	300	300	300	300	D ½, M
Silicon final device layer thickness (tolerance ± 5%) (nm) (Q)	30 - 200	30 - 200	30 - 200	30 - 200	30 - 200	20 - 100	20 - 100	M
Buried oxide (BOX) thickness (tolerance ± 5%) (nm) (R)	≤ 200	≤ 200	≤ 200	≤ 200	≤ 200	≤ 100	≤ 100	M
D_{BOX}, BOX defects (DRAM) (cm^{-2}) (S)	≤ 0.106	≤ 0.100	≤ 0.096	≤ 0.091	≤ 0.085	≤ 0.080	≤ 0.069	D ½
D_{BOX}, BOX defects (MPU) (cm^{-2}) (S)	≤ 0.359	≤ 0.346	≤ 0.352	≤ 0.344	≤ 0.275	≤ 0.254	≤ 0.208	M
D_{INC}, inclusions (DRAM) (cm^{-2}) (T)	≤ 0.127	≤ 0.120	≤ 0.115	≤ 0.109	≤ 0.102	≤ 0.096	≤ 0.082	D ½
D_{INC}, inclusions (MPU) (cm^{-2}) (T)	≤ 0.431	≤ 0.415	≤ 0.422	≤ 0.413	≤ 0.330	≤ 0.305	≤ 0.250	M
D_{TD}, threading dislocations (DRAM,MPU) (cm^{-2}) (U)	≤ 2 x 10^6	≤ 2 x 10^6	≤ 2 x 10^6	≤ 2 x 10^6	≤ 2 x 10^6	≤ 2 x 10^6	≤ 2 x 10^6	D ½, M

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

** Parameters define limit values; independent predictors of yield, mathematically or empirically modeled at 99%. limit values rarely coincide for more than one parameter. A given wafer will generally not exhibit more than one limit value "at a time;" other parameter values most likely near median value, thereby ensuring total yield for all parameters is at least 99%.*

*** Significant gaps in metrology and wafer manufacturing equipment need to be closed on 200 mm, especially for the 180 nm and 130 nm nodes, inasmuch as 300 mm ~~is being~~ was delayed and 200 mm will still be prevalent at the 130 nm node.*

**** Numerical values are for 300 mm, although 200 mm will be the dominant polished and epitaxial wafer diameter.*

***** Edge exclusion = 3 mm is consistent with equipment and wafer fab capabilities through 2002. Reduction in the edge exclusion beyond 2002 is desirable to increase chips per wafer.*

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

A. Widespread industry practice indicates the introduction of scaled DRAM 1/2 pitches and MPU/ASIC gate lengths that are smaller than forecasted in the 1999 ITRS.

These proposed 1/2 pitch values are presented here. The table values have not been changed to reflect these new proposed 1/2 pitch values.

B. Organics/polymers modeled approximately 0.1 of a monolayer, £ 1E+14 C at/cm^2. Surface organic levels are highly dependent on wafer packaging, on hydrophobic or hydrophilic wafer surface conditions, and on wafer storage conditions such as temperature, time and ambient.

C. Front-surface microroughness £ 0.10 nm (RMS) for all CD generations; instrumentation choice, target values, and spatial frequency range (scan size) are selected based on application. Power spectral density analysis is recommended to utilize full accessible range of instruments.

D. Front surface particle or crystal originated pit (COP) size = K_1(CD); K_1 = 0.5 for design rules smaller than 130 nm. For design rules ³ 130 nm, the particle or COP size = K_{11}, where K_{11} = 90 nm. Optical particle counters are believed to report localized scattering event (LSE) signals low by about 10% due to PSL calibration factors which also reduce particle/COP discrimination accuracy. The relationship between actual defect size and associated LSE signal depends on defect type and scanner geometry. COPs are reported larger, metal and semiconductor particles, smaller, and dielectric particles, about the same as LSE signals. One solution is defect sizing based on defect identification. Relating defect size to yield is difficult since defects are not correctly sized. State-of-the-art LSE capability is judged to be 90 nm through 2002.

E. Front-surface particles modeled for 99% yield by $Y = \exp[-D_P R_P T a (CD)^2]$ (1), R_P = 0.2, T = # of transistors or bits/chip per technology generation, and a is the DRAM cell area factor, a function of the technology generation. Assuming a pre-gate cleaning efficiency of 50% for particles in Surface Preparation, the particle values are accordingly increased by a factor 2. This results in a number twice that listed in the Surface Preparation values in Table 33. The analogous a value for MPUs is not available, so the MPU

particles are taken equal to the DRAM values.

Detailed back-surface particle information is not included in Table 32a, since, in practice, lithography concerns are being met by identifying back-surface particles visually, suggesting that only large defects are of impact. If desired, the calculations may be made using the following models for back-surface particle size and density.

The front-surface height elevation, H, due to a back-surface particle of size, D, under a back-surface film of thickness, T, and a wafer thickness, W, may be expressed as [(xD +xT +W) - (T + W)], which may be reduced to [(xD) - (1-x)T], where x = 0.6 is the compression of the particle and back-surface film due to the pressure of the chuck on the wafer. Assuming a front-surface elevation of 2(CD) results in a 100% lithographic printing failure, the back-surface particle size is expressed as: D = [(2/0.6) (CD) + (0.4/0.6) (T)], where CD and T are expressed in nm. In this model, T may be set equal to 100 nm, for example.

Back-surface particles modeled for 99% yield: $Y = \exp[-D_P R_P A_{eff}]$ (1). R_P = 1.0, $A_{eff} = A_{CHIP} \times 0.03 \times 0.8$, where 0.03 corresponds to 3% of the chip area touching the chuck and 0.8 corresponds to 80% of the effective chip area that is degraded by effects of the back-surface particle on the front-surface de-focus effect. Dp, then, represents the density of defects allowable in visible inspection for back-side particles. See Tables 1a and 1b for the chip areas.

F. DRAM cell "a" factor forecasts published in the 1999 ITRS were determined to be too aggressive. New proposed DRAM "a" factor forecasts are presented in Table 1a, which will change the effective DRAM areas utilized in the yield calculations. The table values have not been changed to reflect these new values.

G. Metals empirically modeled for 99% yield by $Y = \exp[-D_M R_M T a (CD)^2]$ (1), R_M =0.2, T = # of transistors or bits/chip per technology generation and "a" is the DRAM cell area factor, a function of the technology generation, with $D_M = K_2 (M)^3 \exp[-T_o/0.7]$, K_2= 1.854 ´ 10^{-29} cm^4, T_o equivalent oxide thickness (corrected for quantum mechanical and poly depletion effects), in nm per technology generation (based on MIS DRAM device structure). The experimental data resulting in this model is based on and extends the precursor publication (2). Assuming a pre-gate cleaning efficiency of 50% for metals in Surface Preparation, the metal values are accordingly increased by a factor 2. This results in a number twice that listed in the Surface Preparation values in Table 21. The value listed is the limit for each of the following metals: Ca, Co, Cu, Cr, Fe, K, Na and Ni.

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2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

H. The metric for site flatness should be matched to the type of exposure equipment used in leading edge applications. For the 180 nm technology node, full-field steppers with square fields (nominally 22 ´ 22 mm) will be utilized and SFQR is the appropriate metric. For the 130 nm technology node to the end of optical lithography, scanners will be utilized with rectangular fields (nominally 25 mm ´ 32 mm) and SFSR is the appropriate metric. In either case, the metric value is approximately equal to the CD for dense lines (DRAM half pitch). Partial sites should be included. Note that flatness metrology requires sufficient spatial resolution to capture topographical features relevant for each technology node. This can be expressed as a bandwidth, defined as the upper spatial frequency corresponding to a specified attenuation level. Work is being done in a task force of the SEMI Global Silicon Wafer Committee (PRECOM-1) to validate the methodology and to determine appropriate values.

I. Range of center-point value based on IC requirements. ± tolerance is min-max range about center-point value. Bulk Micro Defects (BMD) for internally gettered or not internally gettered polished wafer > 1 ´ 10^8/cm^3 or < 1 ´ 10^7/cm^3, respectively, after IC processing. The IOC '88 oxygen concentration value is obtained by multiplying the ASTM F121-79 value by 0.652 (See ASTM Test Method F1188-00 for conversion and calibration factors). METROLOGY NOTE: P/T ratios of current measurement techniques (GFA, SIMS, FTIR) for oxygen in heavily doped silicon are inadequate to assure a tolerance of ± 2 ppma. General agreement on a single calibration factor for use in determination of oxygen by IR absorption spectroscopy is needed.

J. COPs modeled for 99% yield by $Y = exp [-D_C R_C T a (CD)^2] (1)$, $R_C = 0.1$, T = # of transistors or bits/chip per technology generation and "a" is the DRAM cell area factor, a function of the technology generation. The analogous "a" value for MPUs is uncertain, so the MPU COPs are taken equal to the DRAM values.

K. Fe consistent with recombination lifetime, t_r, as measured by the SPV technique at low injection level (3). Note that the bulk Fe concentration (at/cm^3) cannot be converted to surface concentration (at/cm^2) via wafer thickness. Recombination lifetime, t_r ³ 2 $(L^2)/D_n$, where L = minority-carrier diffusion length and D_n = minority-carrier diffusion coefficient at 27°C (4). The diffusion length is taken equal to the wafer thickness and a safety factor of 2 is used. Appropriate technique(s) to control, stabilize and passivate surface effects required, depending on the technique (SPV, PCD, etc.) No oxygen precipitation in sample, no back-side mechanical damage, and resistivity of 5–20 ohm-cm recommended.

L. OSF density empirically modeled by $K_3 (CD)^{1.42}$; CD in nm; K_3 = 2.75 ´ 10^{-3} (5); test at 1100°C, 1 hour steam, strip oxide/etch; n-type material more difficult to control OSF

M. Other epitaxial defects such as hillocks and mounds should also be accounted for, but an appropriate yield model is not available.

N. Desired epitaxial layer thickness tolerance is ± 4% for a 2 to 10 mm center-point epitaxial layer thickness target value.

O. Large area epitaxial defects modeled at 99% yield where $Y = exp [-D_{LAD} R_{LAD} A_{CHIP}] (1)$, where $R_{LAD} = 1$ and A_{CHIP} applies to DRAM and MPU as appropriate. Large area epitaxial defects are defined as having an LSE signal ³ 1.0 mm. See Tables 1a and 1b, pages A-3 to A-6, for the chip areas utilized. Starting Materials uses the DRAM at production and the MPU high volume/low performance areas per the most recent ORTC inputs. METROLOGY NOTE: Many current generation scanning surface inspection systems (SSIS) cannot reliably size surface features with LSE signals greater than about 0.5 mm due to the light scattering characteristics of these large structural epi defects and the optical design of the tool. Further, a metrology gap clearly exists since production worthy tools are not available that can separate large structural epi defects from other features like large particles.

P. Epitaxial stacking faults modeled at 99% yield where $Y = exp [-D_{SF} R_{SF} A_{CHIP}] (1)$, where $R_{SF} = 0.5$ and A_{CHIP} applies to DRAM and MPU as appropriate. See Tables 1a and 1b, pages A-3 to A-6, for the chip areas utilized. Starting Materials uses the DRAM at production and the MPU high volume/low performance areas per the most recent ORTC inputs. METROLOGY NOTE: A metrology gap clearly exists since production worthy tools are not available that can identify and count epitaxial stacking faults.

Q. Range of target value refers to the center point measurement with tolerance to indicate within-wafer maximum positive or negative % deviation from the center value. The final device silicon is less than incoming material due to consumption during device fabrication. Currently listed values are applicable for both partially- and fully-depleted

films and are the best available data at the present time. For fully depleted films, the silicon and buried oxide (BOX) thicknesses may be equally partitioned.

R. Range of target value refers to the center point measurement with tolerance to indicate within-wafer maximum positive or negative % deviation from the center value. Currently listed values are applicable for both partially- and fully-depleted films and are the best available data at the present time. Top silicon-BOX interface charge <1011/cm^2. For fully depleted films, the silicon and buried oxide (BOX) thicknesses may be equally partitioned.

S. BOX defects with yield of 99%; $Y = exp [-D_{BOX} R_{BOX} T b (CD)^2 d] (1)$, D_{BOX} = BOX defect density (mainly pinholes), R_{BOX} = 0.2 (best present estimate), b = 1 for DRAM and 10 for MPU; d = 6 units (gate, source, and drain [includes LDD extension])

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

T. Inclusions defects with yield of 99%; $Y = \exp [-D_{INC} R_{INC} T b (CD)^2 d]$ (1), D_{INC} = inclusion defect density, R_{INC} = 1 (best present estimate), b = 1 for DRAM and 10 for MPU; d = 1 unit (gate). Test is done using HF etchant (6-8) to decorate defects and subsequent optical counting. Sources of inclusions can include COPs, metal silicides, or local SiO_2 islands in the top silicon layer. These inclusions may also be detected by localized light scattering (LLS) measurements (7-9).

U. Yields comparable to bulk devices have been achieved with threading dislocations, DTD, of 2 ´ 10^6/cm^2. Kill ratios are not sufficiently known for reliable calculations; experimental yield/DTD correlation data must be obtained. Downward trends in DTD for future technology generations are expected.

1. W. Maly, H.T. Heineken, and F. Agricola. "A Simple New Yield Model." Semiconductor International, number 7, 1994, pages 148–154.

2. W.B. Henley, L. Jastrzebski and N.F. Haddad, The Effects of Iron Contamination on Thin Oxide Breakdown-Experimental and Modeling, MRS 262, 993–998 (1992)

3. G. Zoth and W. Bergholtz, "A Fast, Preparation-Free Method to Detect Iron in Silicon," J. Appl. Phys. Vol. 67, P. 6764-6771, June 1990.

4. M. Kamoshida. "Trends of Silicon Wafer Specifications vs. Design Rules in ULSI Device Fabrication. Particles, Flatness and Impurity Distribution Deviations." DENKA KAGAKU, number 3, 1995, pages 194–204.

5. W. Shockley, Electrons and Holes in Semiconductors, p.69, Princeton: D. Van Nostrand Co., Inc. 1950.

6. Y. Omura, S. Nakashima, K. Izumi, and T. Ishii. "0.1-um-Gate, Ultrathin-Film CMOS Devices Using SIMOX Substrate with 80-nm-Thick Buried Oxide Layer." IEDM Technical Digest, pp.675–678, 1991.

7. D.K. Sadana, J. Lasky, H.J. Hovel, K. Petrillo and P. Roitman. "Nano-Defects in Commercial Bonded SOI and SIMOX." 1994 IEEE International SOI Conference Proceedings, pp. 111–1112, Nantucket Island, MA (1994).

8. W. P. Maszara, R. Dockerty, C.F.H. Gondran and P.K. Vasudev. "SOI Materials for Mainstream CMOS Technology." in Silicon-On-Insulator Technology and Devices VIII, X. Cristoloveanu, P.L.F. Hemment, K. Izumi and S. Wilson editors, PV 97-23, pp. 15–26, The Electrochemical Society Proceeding Series, Pennington, NJ (1997).

9. H. Aga, M. Nakano and K. Mitani. "Study of HF Defects in Thin Bonded SOI Dependent on Original Wafers." Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, pp. 304–305, Hiroshima (1998).

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All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

*Table 32b Starting Materials Technology Requirements—Long Term***

Year of First Product Shipment *Technology Node*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	*Driver*
Proposed Year of First Product Shipment, Technology Node (A)	***2008 60nm***	***2011 40 nm***	***2014 30 nm***	*Driver*
DRAM 1/2 Pitch (nm)	**70**	**50**	**35**	**D ½**
New DRAM 1/2 Pitch (nm) (A)	**60**	**40**	**30**	**D ½**
MPU Gate Length (nm)	**45**	**32**	**22**	**M**
New MPU/ASIC Gate Length (In Resist) (nm) (A)	**45**	**33**	**23**	**M**
General Characteristics * (B,C)				
Wafer diameter (mm)	**300**	**300**	**450**	**D ½,M**
Edge exclusion (mm)	**1**	**1**	**1**	**D ½,M**
Front surface particle size (nm), latex sphere equivalent (D)	≥ 35	≥ 25	≥ 17.5	***D ½,M***
Particles (cm^{-2}) (E,F)	≤ 0.10	≤ 0.10	≤ 0.10	***D ½,M***
Particles (#/wf)	≤ 73	≤ 72	≤ 165	***D ½,M***
Critical surface metals (at/cm^2) (G)	≤ 4.2E+9	≤ 3.6E+9	≤ 3.4E+9	**D ½,M**
Site flatness (nm) (H)	≤ 70	≤ 50	≤ 35	***D ½,M***
Oxygen (center point value ± 2.0 ppma) (ASTM '79) (I)	**18–31**	**18–31**	**18-31**	**D ½,M**
Polished Wafer *				
Total Allowable Front Surface Light Scattering Defect Density is The Sum of Crystal Originated Pits (COPs) and Particles (see General Characteristics)				
Front surface COPs size (nm), latex sphere equivalent (D)	≥ 35	≥ 25	≥ 18	***D ½,M***
COPs (cm^{-2}) (J)	≤ 0.10	≤ 0.10	≤ 0.10	***D ½,M***
COPs (#/wf)	≤ 73	≤ 72	≤ 165	***D ½,M***
Total bulk Fe (at/cm^3) (K)	**< 1 x 10^{10}**	**< 1 x 10^{10}**	**< 1 x 10^{10}**	**D ½,M**
Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) (L)	≤ 1.1	≤ 0.7	≤ 0.4	**D ½**
Oxidation stacking faults (OSF) (MPU) (cm^{-2}) (L)	≤ 0.6	≤ 0.4	≤ 0.2	**M**
Epitaxial Wafer *				
Total Allowable Front Surface Defect Density is The Sum of Epitaxial Large Area Defects, Epitaxial Stacking Faults and Particles (see General Characteristics) (M,N)				
Layer large area defects (DRAM) (cm^{-2}) (O)	≤ 0.005	≤ 0.004	≤ 0.004	**D ½**
Layer large area defects (MPU) (cm^{-2}) (O)	≤ 0.006	≤ 0.006	≤ 0.006	**M**
Layer stacking faults (DRAM) (cm^{-2}) (P)	≤ 0.010	≤ 0.009	≤ 0.008	**D ½**
Layer stacking faults (MPU) (cm^{-2}) (P)	≤ 0.012	≤ 0.012	≤ 0.012	**M**

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION *TECHNOLOGY NODE* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
YEAR OF PRODUCTION *TECHNOLOGY NODE* ***(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

*Table 32b Term Starting Materials Technology Requirements—Long Term(continued)***

Year of First Product Shipment *Technology Node*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	*Driver*
Proposed Year of First Product Shipment, Technology Node (A)	***2008*** ***60nm***	***2011*** ***40 nm***	***2014*** ***30 nm***	
DRAM 1/2 Pitch (nm)	**70**	**50**	**35**	**D ½**
New DRAM 1/2 Pitch (nm) (A)	***60***	***40***	***30***	***D ½***
MPU Gate Length (nm)	**45**	**32**	**22**	**M**
New MPU/ASIC Gate Length (In Resist) (nm) (A)	***45***	***33***	***23***	***M***
Silicon-On-Insulator Wafer*				
Wafer diameter (mm)	***300***	***300***	***450***	***D ½, M***
Silicon final device layer thickness (tolerance ± 5%) (nm) (Q)	**20 - 100**	**20 - 100**	**20 - 100**	**M**
Buried oxide (BOX) thickness (tolerance ± 5%) (nm) (R)	≤ 70	≤ 50	≤ 50	**M**
D_{BOX}, BOX defects (DRAM) (cm^{-2}) (S)	≤ 0.061	≤ 0.060	≤ 0.052	**D ½**
D_{BOX}, BOX defects (MPU) (cm^{-2}) (S)	≤ 0.154	≤ 0.107	≤ 0.080	**M**
D_{INC}, inclusions (DRAM) (cm^{-2}) (T)	≤ 0.073	≤ 0.072	≤ 0.063	**D ½**
D_{INC}, inclusions (MPU) (cm^{-2}) (T)	≤ 0.184	≤ 0.129	≤ 0.096	**M**
D_{TD}, threading dislocations (DRAM,MPU) (cm^{-2}) (U)	**≤ 2 x 10^6**	**≤ 2 x 10^6**	**≤ 2 x 10^6**	**D ½, M**

** Parameters define limit values; independent predictors of yield, mathematically or empirically modeled at 99%. limit values rarely coincide for more than one parameter. A given wafer will generally not exhibit more than one limit value "at a time;" other parameter values most likely near median value, thereby ensuring total yield for all parameters is at least 99%.*

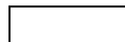
*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

*Table 33a Surface Preparation Technology Requirements—Near Term***

Proposed Year of Introduction, Technology Node (*)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90 nm**	2005	Driver
Front End of Line (A)								
DRAM critical area (cm^2) (B) (*)	0.32	0.32	0.68	0.68	0.68	1.6	1.6	D 1/2
Logic critical area (cm^2) (C)	0.1	0.1	0.13	0.13	0.13	0.19	0.19	M
DRAM GOI D_0 (cm^{-2}) (D)	0.03	0.03	0.01	0.01	0.01	0.01	0.01	***D 1/2***
Logic GOI D_0 (cm^{-2}) (D)	0.10	0.10	0.08	0.08	0.08	0.05	0.05	***M***
Light scatterers, front side (E)								
DRAM (cm^{-2})	0.064	0.06	0.058	0.068	0.064	0.06	0.051	D 1/2
Logic (cm^{-2})	0.064	0.06	0.058	0.068	0.064	0.06	0.051	M
Particle size (nm)	90	82.5	75	65	60	55	50	D 1/2
Light scatterers, back side (cm^{-2}) (F)	0.315	0.325	0.290	0.275	0.265	0.250	0.240	D 1/2
Particle size (nm) (F)	500	450	400	333	300	267	233	D 1/2
Critical surface metals (at/cm^2) (G)	$\leq 9 \times 10^9$	$\leq 7 \times 10^9$	$\leq 6 \times 10^9$	$\leq 4.4 \times 10^9$	$\leq 3.4 \times 10^9$	$\leq 2.9 \times 10^9$	$\leq 2.5 \times 10^9$	D 1/2
Mobile ions (atoms/cm^2) (H)	4.25E+10	4.25E+10	4.70E+10	4.70E+10	4.70E+10	4.68E+10	4.7E+10	M / D 1/2
Organics/polymers (C atoms/cm^2) (J)	7.3E+13	6.6E+13	6.0E+13	5.3E+13	4.9E+13	4.5E+13	4.1E+13	M / D 1/2
Surface Oxygen (O atoms/cm^2) (K)	<1E+14	<1E+14	<1E+14	<1E+14	<1E+14	<1E+14	<1E+12	M / D 1/2
Surface Roughness (nm) (L)	0.15	0.14	0.13	0.12	0.12	0.1	0.1	M / D 1/2
DRAM Water Marks (/cm^2) (M)	2.50E-03	2.27E-03	2.03E-03	1.80E-03	1.63E-03	1.45E-03	1.28E-03	D 1/2
Logic Water Marks (/cm^2) (M)	2.79E-03	2.64E-03	2.49E-03	2.34E-03	2.20E-03	2.07E-03	1.93E-03	M
Back End of Line (N)								
Particles (cm^{-2}) (O)	0.064	0.06	0.058	0.068	0.064	0.06	0.051	M
Particle size (nm)	180	165	150	130	120	110	100	M
Corrosion Resistance (P)	>10 years	>10 years	>10 years	>10 years	>10 years	>10 years	>10 years	M
Surface Oxygen (O atoms/cm2) (K)	<1E+14	<1E+14	<1E+14	<1E+14	<1E+14	<1E+14	<1E+12	M

Solutions Exist  *Solutions Being Pursued* *No Known Solution*

**** Widespread industry practice indicates the introduction of scaled DRAM 1/2-pitches that are smaller than forecasted in the 1999 ITRS. These proposed 1/2-pitch values are presented here. The table values have not been changed to reflect these new proposed 1/2-pitch values.***

Other footnotes remain unchanged

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 33b Surface Preparation Technology Requirements—Long Term***

Proposed Year of Introduction Technology Node (*)	*2008 60 nm*	*2011 40 nm*	*2014 30 nm*	*Driver*
Front End of Line (A)				
DRAM critical area (cm^2) (B) (*)	3.14	6.4	6.4	D 1/2
Logic critical area (cm^2) (C)	0.24	0.43	0.43	M
DRAM GOI D_0 (cm^{-2}) (D)	0.003	0.002	0.002	***D 1/2***
Logic GOI D_0 (cm^{-2}) (D)	0.042	0.023	0.023	***M***
Light scatterers, front side (E)				
DRAM (cm^{-2})	0.052	0.052	0.052	D 1/2
Logic (cm^{-2})	0.052	0.052	0.052	M
Particle size (nm)	35	25	18	D 1/2
Light scatterers, back side (F)	0.210	0.185	0.160	D 1/2
Particle size (nm)	133	67	17	D 1/2
Critical surface metals (at/cm^2) (G)	$\leq 2.1 \times 10^9$	$\leq 1.8 \times 10^9$	$\leq 1.7 \times 10^9$	D 1/2
Mobile ions ($atoms/cm^2$) (H)	4.4E+10	4.5E+10	6.0E+10	M / D 1/2
Organics/polymers (C $atoms/cm^2$) (J)	2.8E+13	2.0E+13	1.4E+13	M / D 1/2
Surface Oxygen (O $atoms/cm^2$) (K)	<1E+12	<1E+12	<1E+12	M / D 1/2
Surface Roughness (nm) (L)	0.08	0.08	0.08	M / D 1/2
DRAM Water Marks ($/cm^2$) (M)	9.02E-04	4.51E-04	6.39E-04	D 1/2
Logic Water Marks ($/cm^2$) (M)	1.63E-03	1.35E-03	1.12E-03	M
Back End of Line (N)				
Particles (cm^{-2}) (O)	0.052	0.052	0.052	M
Particle size (nm)	70	50	36	M
Corrosion Resistance (P)	>10yrs.	>10 YRS.	>10 YRS.	M
Surface Oxygen (O atoms/cm2) (K)	<1E+12	<1E+12	<1E+12	M

Solutions Exist *Solutions Being Pursued* *No Known Solution*

***** Widespread industry practice indicates the introduction of scaled DRAM 1/2-pitches that are smaller than forecasted in the 1999 ITRS. These proposed 1/2-pitch values are presented here. The table values have not been changed to reflect these new proposed 1/2-pitch values.***

Other footnotes remain unchanged

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

*Table 34a Thermal/Thin Films, Gate Etch, and Doping Technology Requirements—Near Term***

Proposed Year of First Product Shipment ***Technology Node (A1)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90 nm***	*2005*	*Driver*
*MPU/**ASIC** Gate Length (nm)*	***120***	***100***	***90***	***85-90***	*80*	*70*	*65*	***MPU/ASIC***
Final Physical Bottom Gate Length after Etch, Proposed (nm)[A2]	***120***	***100***	***90***	***80***	***70***	***65***	***60***	***MPU/ASIC***
Equivalent physical oxide thickness T_{ox} (nm) [A]	**1.9–2.5**	***1.5-1.9***	**1.5–1.9**	**1.5–1.9**	**1.5–1.9**	**1.2–1.5**	**1.0–1.5**	***MPU/ASIC***
Gate dielectric leakage at 100°C (nA/µm) High-performance [B]	**7**	**8**	**10**	**10**	**13**	**16**	**20**	***MPU/ASIC***
Gate dielectric leakage at 100°C (pA/µm) low power [B]	**7**	***8***	***10***	**10**	**13**	**16**	**20**	***MPU/ASIC***
Thickness control EOT (% 3σ) [C]	**<± 4**	**<± 4**	**<± 4**	**<± 4**	**<± 4**	**<± 4**	**<± 4**	***MPU/ASIC***
Leffective control	**≤ 20%**	***≤ 20%***	**≤ 20%**	**≤ 20%**	**≤ 20%**	**≤ 20%**	**≤ 20%**	***MPU/ASIC***
L_{gate} 3σ variation (nm) (dense and isolated lines) [D]	***12***	***10***	***8.5***	**8.5**	**8**	**7**	**6.5**	***MPU/ASIC***
CD bias between dense and isolated lines [E]	**≤ 15%**	**≤ 15%**	**≤ 15%**	**≤ 15%**	**≤ 15%**	**≤ 15%**	**≤ 15%**	***MPU/ASIC***
Minimum measurable gate dielectric remaining (post gate etch clean) [F]	**>0**	**>0**	**>0**	**>0**	**>0**	**>0**	**>0**	***MPU/ASIC***
Sidewall spacer thickness (nm) extension structure [G]	***65-130***	***59-108***	***52-104***	**52–104**	**48–96**	**44–88**	**40–80**	***MPU/ASIC***
Sidewall spacer thickness (nm) elevated contact [H]	—	—	—	—	—	—	**20–40**	***MPU/ASIC***
Sidewall spacer thickness (nm) single drain [I]	—	—	—	—	—	—	—	***MPU/ASIC***
Sidewall spacer thickness control (nm, 3σ)	**≤ 10%**	***≤ 10%***	**≤ 10%**	**≤ 10%**	**≤ 10%**	**≤ 10%**	**≤ 10%**	***MPU/ASIC***

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

*Table 34a Thermal/Thin Films, Gate Etch, and Doping Technology Requirements—Near Term (continued)***

Proposed Year of First Product Shipment ***Technology Node (A1)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90 nm***	*2005*	*Driver*
*MPU/**ASIC** Gate Length (nm)*	***120***	***100***	***90***	***85-90***	*80*	*70*	*65*	***MPU/ASIC***
Final Physical Bottom Gate Length after Etch, Proposed (nm)[A2]	***120***	***100***	***90***	***80***	***70***	***65***	***60***	***MPU/ASIC***
Gate electrode sheet Rs (Ω/□) [J]	4–6	4–6	4–6	4–6	4–6	4–6	4–6	***MPU/ASIC***
Gate electrode thickness [K]	***120***	***100***	***85***	85	80	70	65	***MPU/ASIC***
Gate electrode resistivity (μΩ-cm) [L]	***60***	***50***	***43***	43	40	35	33	***MPU/ASIC***
Active poly doping to achieve 10% GOx depletion [M]	2.2×10^{20}	***3.1×10^{20}***	3.1×10^{20}	3.1×10^{20}	3.1×10^{20}	3.9×10^{20}	4.6×10^{20}	***MPU/ASIC***
Contact silicide sheet Rs (Ω/□) [O]	***3.3***	***3.8***	***4.4***	4.4	4.7	5.4	6.0	***MPU/ASIC***
Contact maximum resistivity (Ω-cm^2) [P]	***$< 2.5\times10^{-7}$***	***$< 2.0\times10^{-7}$***	***$<1.7\times10^{-7}$***	$<1.7\times10^{-7}$	$<1.6\times10^{-7}$	$<1.1\times10^{-7}$	$<1.0\times10^{-7}$	***MPU/ASIC***
Maximum silicon consumption (nm) [Q]	***32-60***	***26-50***	***22-43***	22–43	20–40	18–36	16–33	***MPU/ASIC***
Contact Xj (nm) [R]	***65-125***	***55-105***	***45-90***	45–90	43–85	38–75	35–70	***MPU/ASIC***
Drain extension Xj (nm) [S]	***36-60***	***30-50***	***25-43***	25–43	24–40	20–35	20–33	***MPU/ASIC***
Drain extension sheet resistance (Ω/□)	***310-760***	***280-730***	***250-700***	250–700	240–675	220–650	200–625	***MPU/ASIC***
Lateral abruptness for source extension (nm/decade) [T]	***4.1***	***3.4***	***2.9***	2.9	2.7	2.4	2.2	***MPU/ASIC***
Extension lateral abruptness (nm/decade) [U]	***12***	***10***	***8.5***	8.5	8	7	6.5	***MPU/ASIC***
Potential: dopant variation—Position (nm)	***10***	10	10	<10	<8	<8	<7	***MPU/ASIC***
Potential: dopant variation—Dose	<10% (Halo)	***<9% (Halo)***	***<8%***	<8%	<7%	<6%	<5%	***MPU/ASIC***
Channel concentration for W depletion <1/4L_{eff} (cm^{-3}) [V]	***2.3×10^{18}***	***2.7×10^{18}***	***3.0×10^{18}***	3.0×10^{18}	3.3×10^{18}	3.7×10^{18}	4.0×10^{18}	***MPU/ASIC***
Uniform channel concentration (cm^{-3}), for V_t=0.4 [W]	0.8–1.5×10^{18}	***1.5–2.5×10^{18}***	1.5–2.5×10^{18}	1.5–2.5×10^{18}	1.5–2.5×10^{18}	2.5–4.0×10^{18}	2.5–6.0×10^{18}	***MPU/ASIC***
Retrograde Channel Depth (nm) [X]	***< 18-30***	***< 15-25***	***< 12-22***	< 12–22	<12–20	< 10–18	< 10–17	***MPU/ASIC***

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 34b Thermal/Thin Films, Gate Etch, and Doping Technology Requirements for Logic—Long Term***

YEAR TECHNOLOGY NODE (A1)	2008 60 nm	2011 40 nm	2014 30 nm	DRIVER
MPU/ASIC Gate Length (nm)	45	32	22	MPU/ASIC
Final Physical Bottom Gate Length after Etch, Proposed (nm)[A2]	41	29	20	MPU/ASIC
Equivalent physical oxide thickness T_{ox} (nm) [A]	0.8–1.2	0.6–0.8	0.5–0.6	MPU/ASIC
Gate dielectric leakage at 100°C (nA/µm) high-performance [B]	40	80	160	MPU/ASIC
Gate dielectric leakage at 100°C (pA/µm) low power [B]	40	80	160	MPU/ASIC
Thickness control EOT (% 3σ) [C]	<± 4	<± 4	<± 4	MPU/ASIC
Leffective control	≤ 20%	≤ 20%	≤ 20%	MPU/ASIC
L_{gate} 3σ variation (nm) (dense and isolated lines) [D]	5	3.2	2.2	MPU/ASIC
CD bias between dense and isolated lines [E]	≤ 15%	≤ 15%	≤ 15%	MPU/ASIC
Minimum measurable gate dielectric remaining (post gate etch clean) [F]	>0	>0	>0	MPU/ASIC
Sidewall spacer thickness (nm) extension structure [G]	28–56	20–40	14–28	MPU/ASIC
Sidewall spacer thickness (nm) elevated contact [H]	14–28	10–20	7–14	MPU/ASIC
Sidewall spacer thickness (nm) single drain [I]	7.5–15	5–10	3.7–7.5	MPU/ASIC
Sidewall spacer thickness control (nm, 3σ)	≤ 10%	≤ 10%	≤ 10%	MPU/ASIC
Gate electrode sheet Rs (Ω/□) [J]	4–6	4–6	4–6	MPU/ASIC
Gate electrode thickness [K]	45	32	22	MPU/ASIC
Gate electrode resistivity (µΩ-cm) [L]	23	16	11	MPU/ASIC
Active poly doping to achieve 10% Gox depletion [M]	5.4×10^{20}	7.3×10^{20}	1.2×10^{21}	MPU/ASIC

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 34b Thermal/Thin Films, Gate Etch, and Doping Technology Requirements for Logic—Long Term (continued)**

YEAR TECHNOLOGY NODE (A1)	2008 60 nm	2011 40 nm	2014 30 nm	DRIVER
MPU/ASIC Gate Length (nm)	45	32	22	MPU/ASIC
Final Physical Bottom Gate Length after Etch, Proposed (nm)[A2]	41	29	20	MPU/ASIC
Silicide thickness (nm) [N]	20	15	12	MPU/ASIC
Contact silicide sheet Rs (Ω/□) [O]	7.5	10.0	12.5	MPU/ASIC
Contact maximum resistivity (Ω-cm^2) [P]	< 5.0×10^{-8}	< 2.5×10^{-8}	< 1.5×10^{-8}	MPU/ASIC
Maximum silicon consumption (nm) [Q]	14–26	10–19	7–17	MPU/ASIC
Contact Xj (nm) [R]	30–55	20–40	15–35	MPU/ASIC
Drain extension Xj (nm) [S]	16–26	11–19	8–13	MPU/ASIC
Drain extension sheet resistance (Ω/□)	150–525	120–450	100–400	MPU/ASIC
Lateral abruptness for source extension (nm/decade) [T]	1.25	0.8	0.5	MPU/ASIC
Extension lateral abruptness (nm/decade) [U]	4.5	3.2	2.2	MPU/ASIC
Potential: dopant variation—position (nm)	<5	<4	<3	MPU/ASIC
Potential: dopant variation—dose	5.0×10^{-2}	3.0×10^{-2}	2.0×10^{-2}	MPU/ASIC
Channel concentration for Wdepletion <1/4L_{eff} (cm^{-3}) [V]	8.0×10^{18}	1.4×10^{19}	3×10^{19}	MPU/ASIC
Uniform.. channel conc. (cm^{-3}), for V_t=0.4 [W]	4.0–9.0×10^{18}	0.9–1.5×10^{19}	1.5–2.5×10^{19}	MPU/ASIC
Retrograde channel depth (nm/decade) [X]	< 8–13	< 5–10	< 4–8	MPU/ASIC

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

Notes for Table 34a and b Thermal / Thin Films, Gate Etch, and Doping Requirements

[A1] Widespread industry practice indicates the introduction of scaled DRAM ½ pitches that are smaller than forecasted in the 1999 ITRS. These proposed ½ pitch values are presented here. The table values have not been changed to reflect these new proposed ½ pitch values.

[A2] Widespread industry practice indicates the use of processes that result in physical gate lengths that are smaller than the feature size printed in resist. This proposed gate length is presented here. The table values have not been changed to reflect this new proposed gate length.

[A] This number represents the effective thickness of the dielectric alone, at the maximum operating frequency of the technology, without substrate or electrode effects, and is determined through an electrical measurement of capacitance corrected for substrate and electrode effects.

[B] The gate leakage, specified at 100°C, is taken to be less than or equal to 1% of the transistor off-state leakage at that temperature. This leakage is the same as the Process Integration chapter specifies (Table 28) off-state leakage (excluding the gate leakage component) at room temperature since the device subthreshold leakage and junction leakage components of leakage are expected to increase by a factor of 100× between room temperature and 100°C. This gate leakage is measured on the minimum nominal device, and the specification is taken to apply to all transistor bias configurations, that is, both when $V_g = V_s = 0$ and $V_d = V_{dd}$ as well as when $V_s = V_d \approx 0$ and $V_g = V_{dd}$.

[C] See reference. [6]

[D] The technical challenges related to etch are device structure dependent. A conventional MOS structure is assumed. If other integration schemes, such as the replacement gate, become the preferred approach, the details outlined in this table will have to be updated.

[E] The 10% CD budget is a combined number for lithography, etch, and metrology. No effort is being made to partition the contribution from each. It is believed that both lithography and etch will have to work together to achieve this CD control target.

[F] The need is to have some remaining gate dielectric after the gate etch clean step. Since the dielectric material effectively reduces between technology nodes, the ability of the etch system to stop on that dielectric becomes more difficult. In addition, the metrology capability to measure or detect remaining gate dielectric material is suspect for very small thicknesses.

[G] Sidewall spacer thickness = 0.94 × MPU physical gate length (with a range of about ±33%) for a contacting junction that is 0.94 × MPU physical gate length. Validity established using response surface methodology in A. Srivastava and C.M. Osburn. "Response surface based optimization of 0.1 µm PMOSFETs with Ultra-Thin Gate Dielectrics." [7]

[H] Sidewall spacer thickness = = 0.46 × MPU physical gate length (with a range of about ±33%).

[I] Sidewall spacer thickness = ½ of average extension junction depth (with a range of ±33%); the number was chosen to allow for lateral diffusion of the extension junction beneath the spacer.

[J] Continuation of the historical trend

[K] Taken as MPU physical gate length from aspect ratio considerations

[L] From the sheet resistance and film thicknesses requirements (average); assumes metal gate electrode at and beyond 100nm node.

[M] Poly Activation from a spreadsheet model based on V_{dd} and gate oxide requirements

[N] Silicide thickness should be less than ½ of the center Contact Xj to avoid consumption-induced increase in contact resistivity. [8]

[O] Contact silicide sheet resistance: assumes 15 µΩ-cm silicide resistivity , such as $TiSi_2$ or $CoSi_2$.

[P] Si/Silicide maximum resistivity: numbers based on specification of total parasitic resistance < 10% Rdevice (Vdd/Isat). Spreadsheet used to compute components of parasitic resistance. [9]

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[6] P. Zeitzoff and A. Tasch, "Modeling of Manufacturing Sensitivity and of Statistically Based Process Control Requirements for a 0.18 micron NMOS device," *Characterization and Metrology for ULSI Technology: 1998 International Conference*, D.G. Seiler, et al. eds., page 73.

[7] A. Srivastava and C.M. Osburn, "Response surface based optimization of 0.1 µm PMOSFETs with Ultra-Thin Gate Dielectrics," *SPIE Proc*., vol. 3506, (1998), page 253.

[8] C.M. Osburn, J.Y. Tsai, and J. Sun, "Metal Silicides: Active Elements of ULSI Contacts," *J. Electronic Mater*., vol. 25(11), (1996), page 1725.

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All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE **(1999 ITRS)**	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

[Q] *Silicon consumption assumes formation of cobalt disilicide having silicide thickness/silicon consumption ratios of 0.97.*

[R] *Contact Xj = 0.8×Isolated Line (nm) (with a range of ±33%); based on historical curves. All junction depths measured from x=0 at gate dielectric/silicon interface.*

[S] *Xj at Channel = 0.4×Isolated Line (with a range of about ±25%).*

[T] *S/D Abruptness based on a spreadsheet that emphasizes the spreading resistance impact on total series resistance.* [10]

[U] *Channel abruptness is in nm per decade dropoff in doping concentration = 0.1 * Isolated Line (nm) - based on Short Channel effect* [11]

[V] *Drain extension concentration for W depletion < ¼ Logic Half Pitch (Equation 5-57).* [12]

[W] *Uniform channel concentration for V_t = 0.4* [13]*. Neither quantum mechanical nor potential increase in short channel effects were used in this calculations. These effects do, however, tend to offset each other. The assumption of a constant threshold voltage of 0.4 V may not be consistent with the leakage current criteria. To reach the leakage current criteria may result in unacceptably large threshold voltages for the scaled power supplies resulting in severe performance degradation. In addition, high concentration channels could severely impact drain currents due to impurity scattering.*

[X] *The retrograde well profile must be less than 0.5 × the drain extension depth to improve short channel effects.* [14,15]

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9 C.M. Osburn and K.R. Bellur, "Low Parasitic Resistance Contacts for Scaled ULSI Devices," *Thin Solid Films*, vol. 332, (1998), page 428.

10 K.K. Ng and W.T. Lynch, "Analysis of the Gate-voltage-dependent Series Resistance of MOSFETs," *IEEE Trans. Electron Dev.*, vol. ED-33, (1986), page 965.

11 Y.Taur, "25 nm CMOS Design Considerations," *IEDM 1998, Technical Digest*, IEEE, Dec. 1998, pages 789–792.)

12 B.G. Streetman. "Solid State Electronic Devices," 4th ed., ,. Englewood Cliffs, NJ:Prentice Hall , 1995, page 174.

13 R. Muller and T. Kamins. *Device Electronics for Integrated Circuits*. New York, NY:John Wiley and Sons, Inc., 1977, page 324.

14 S.Thompson, P.Packan, and M.Bohr. "Linear versus Saturated Drive Current: Tradeoffs in Super Steep Retrograde Well Engineering," *VLSI Technology Digest*, (1996), page 154.

15 I.De and C.M. Osborn, "Impact of Super-steep-retrograde Channel Doping Profiles on the Performance of Scaled Devides," *IEEE Trans. Elec. Dev.*, vol. 46, no.8, (1999), page 1711.

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* *(1999 ITRS)*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

*Table35 DRAM Stacked Capacitor Films Technology Requirements***

Year of First Product Shipment *Technology Node*	***1999*** ***180 nm***	***2002*** ***130 nm***	***2005*** ***100 nm***	***2008*** ***70 nm***	***2011*** ***50 nm***	***2014*** ***35 nm***
DRAM Half-Pitch (nm)	**180**	**130**	**100**	**70**	**50**	**35**
Proposed DRAM Half-Pitch for 2001 ITRS (nm) (A)	**180**	**115**	**80**	**60**	**40**	**30**
Cell size factor a (B)	**8.0**	**8.0**	**6.0**	**6.0**	**4.0**	**4.0**
Cell size [um2] (C)	**0.26**	**0.14**	**0.06**	**0.03**	**0.0100**	**0.0050**
	=0.36*0.72	**=0.26*0.52**	**=0.2*0.3**	**=0.14*0.21**	**=0.1*0.1**	**=0.07071*0.07**
Storage Node size [um2] (D)	**0.097**	**0.051**	**0.020**	**0.010**	**0.0025**	**0.0012**
	=0.18*0.54	**=0.13*0.39**	**=0.1*0.2**	**=0.07*0.14**	**=0.05*0.05**	**=0.035355*0.04**
Capacitor Structure	**Cylinder MIS Ta2O5**	**Pedestal MIM Ta2O5 (Ref. U)**	**Pedestal MIM BST**	**Pedestal MIM BST**	**Pedestal MIM epi-BST**	**Pedestal MIM epi-BST**
Dielectric Constant	**22**	**50 Ref. U**	**250**	**250**	**700**	**700**
SN Height H [um]	**0.95**	**0.80**	**0.60**	**0.55**	**0.40**	**0.38**
Cylinder Factor (E)	**1.5**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Roughness Factor	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Total Capacitor Area [um2]	**2.20**	**0.88**	**0.38**	**0.24**	**0.08**	**0.05**
Structural Coefficient (F)	**8.5**	**6.5**	**6.3**	**8.2**	**8.3**	**11.0**
teq@25fF [nm] (G)	**3.0**	**1.22**	**0.52**	**0.33**	**0.11**	**0.08**
t phy.@25fF [nm] (H)	**11.5**	**15.6**	**33.6**	**21.3**	**20.4**	**13.6**
A/R of SN (OUT) for cell plate depo. (I)	**6.0**	**8.1**	**18.3**	**20.1**	**43.9**	**46.9**
HAC diameter [um] (J)	**0.22**	**0.16**	**0.12**	**0.08**	**0.06**	**0.04**
Total interlevel insulator and metal thickness except SN [um] (K)	**1.05**	**0.95**	**0.85**	**0.77**	**0.69**	**0.62**
HAC depth [um] (L)	**2.00**	**1.75**	**1.45**	**1.32**	**1.09**	**1.00**
HAC A/R	**9.3**	**11.2**	**12.1**	**15.7**	**18.1**	**23.6**
Vdd [V] (M)	**1.8**	**1.5**	**1.2**	**0.9**	**0.6**	**0.5**
Retention Time [ms] (N)	**128**	**256**	**512**	**1024**	**2048**	**4096**
Leak Current [fA/cell] (O)	**0.527**	**0.220**	**0.088**	**0.033**	**0.011**	**0.005**
Leak Current Density (nA/cm2)	**24.0**	**24.9**	**23.1**	**13.7**	**13.3**	**8.3**
Deposition Temp. [degree C]	~ 500	~ 500	< 500	< 500	< 500	< 500
Film Anneal Temp. [degree C]	~ 800	~ 750	< 750	~ 650	< 650	< 650
DRAM Gox [nm] (P)	6	5	4	3	2	1.5
Cgate [F/cell] (Q)	**1.9E-16**	**1.2E-16**	**8.6E-17**	**5.6E-17**	**4.3E-17**	**2.9E-17**
Word line Rs [ohm/sq.] (R)	**10**	**8.3**	**6.7**	**5.0**	**3.3**	**2.5**
Cbitline (S)	**1**	**0.80**	**0.68**	**0.53**	**0.42**	**0.33**
Bit line Rs [ohm/sq.] (T)	**10**	**6.5**	**6.1**	**3.8**	**3.7**	**2.3**

(A) In response to observed acceleration of DRAM 1/2 pitch scaling, new proposed values are presented here for year 2001 updating.Table 35 above has not been updated to reflect these new proposed values.

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

(B) a = (Cell size)/F^2 (F : DRAM 1/2 Pitch). New "a" values have been generated for the year 2000 update. Table 35 above has been updated to relect these new "a" values

*(C) Cell size = a*F^2 (Cell shorter side =2F)*

*(D) SN size =(a/2 -1)*F^2 (SN shorter side = F)*

(E) Cylinder structure increase the capa area by a factor of 1.5.

(F) SC = (total Capa area) / (Cell size)

*(G) teq=3.9*E0*(total Capa area)/25fF*

*(H) t phy. = teq*Er/3.9 If polysilicon is used as a bottom electrode. t phy. =(teq-1)*Er/3.9*

(I) A/R of SN (OUT) = (SN height) / (F - 2 t phy.)*

*(J) HAC diameter =1.2*F (HAC : High Aspect Contact)*

(K) The thickness is assumed to be 1.05um@180nm. (10% reduction by each generation)

(L) HAC depth = SN height + Total Interlevel insulator and metal thickness

(M) PIDS Table 14 Min. Logic Vdd (V) (desktop)

(N) DRAM Retention time (PIDS)

*(O) (Sense Limit*C*Vdd/2) / (Retention Time * MARGIN) (Sense limit=30% leak, MARGIN=100)*

(P) FEP Table 22A Equivalent oxide thickness Tox(nm) DRAM

(Q) Gate Area =F^2

(R) Word Line Rs is assumed to be 10ohm/sq. @180nm. (Word Line R)(Cgate) is constant at same WL length.*

(S) Cbitline proportional to F^2/3) (relative value) ; A.Nitayama et al., IEDM Technical Digest, pp. 355-358, 1998.

(T) Bit Line Rs is assumed to be 10ohm/sq. @180nm. (Bit Line R)(Cbitline) is constant when the number of BL cells about 1.4times/BL.*

(U) Koichi Kishiro et al. Jpn. J. Appl. Phys. Vol. 37 (1998) pp. 1336-1339

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All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

*Table36 DRAM Trench Capacitor Films Technology Requirements***

Year of First Product Shipment Technology Node	***1999 180 nm***	***2002 130 nm***	***2005 100 nm***	***2008 70 nm***	***2011 50 nm***	***2014 35 nm***
DRAM Half-Pitch (nm)	180	130	100	70	50	35
DRAM Half-Pitch proposed for 2001 ITRS (nm) (A)	**180**	**115**	**80**	**60**	**40**	**30**
Storage node area, top view [(DRAM 1/2 pitch)^2]	2	2	2	<2	<2	<2
Trench structure	conventi onal	bottled	bottled	bottled	tbd.	tbd.
Trench area enhancement factor	1	1.5	2	2	1.5	1.5
Capacitor dielectric equivalent oxide thickness (nm)	4.5	3.5	3.2	1.5	1	**0.8**
Trench depth [µm], (at 35fF)	6-7	5-6	5-6	4-5	4-5	**4-5**
Aspect ratio (trench depth / trench width)	30-40	40-45	50-60	60-70	>70	>100
Upper electrode	Silicon	Silicon	Silicon	Metal	Metal	Metal
Dielectric material	NO	NO	NO	High-k	High-k	High-k
Bottom electrode	Silicon	Silicon	Silicon	Silicon	Metal	Metal

(A) In response to observed acceleration of DRAM 1/2 Pitch scaling, new proposed values are presented here fore year 2001 updating. Table 36 above has not been updated to reflect these new proposed values.

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.