

International Technology
Roadmap for
Semiconductors
2000 Update

Design

TABLE OF CONTENTS

Design..... 1

 Summary 1

 2000 Update Tables 2

 New Table--Scenario for SoC Productivity** 2

DESIGN

SUMMARY

Design productivity and the productivity gap have long been cited in the ITRS and its predecessors and in other roadmaps as indications of how productivity will have to increase to make use of the ever-growing number of circuits available on a chip. This table expands on that notion and extends it, going a step farther and suggesting possible ways in which the increased density made available along the Moore's law path will be used by designers. We point out that this is not the only scenario for design, but is an attempt at a reasonable path in a particular case.

The assumptions are that for a short time-to-product, small design team effort of a single-chip system, the team size and time-to market cannot grow much. A 10-person team, one-year design cycle is assumed. Design productivity (transistors per designer per month) for new logic is assumed to increase at 30% per year, a number greater than the design productivity number of the "productivity gap" chart but in line with recent figures. Reuse of old designs is not assumed to be free, but is estimated at one-half the effort of new design, with productivity increasing at the same rate. Chip size is assumed to be one square centimeter, but with memory occupying the part of the chip not occupied by the feasible design effort.

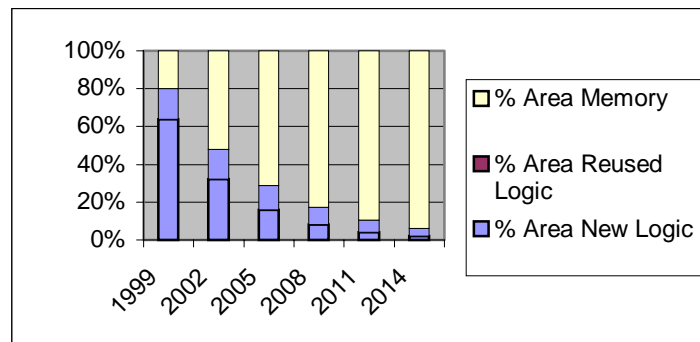
It is important to note that in the result, the absolute number of logic transistors increases greatly, despite the fact that the portion of the chip occupied by new and reused logic decreases to less than 10% of the available area.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE <i>(1999 ITRS)</i>	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE <i>(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)</i>	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

2000 UPDATE TABLES

*New Table--Scenario for SoC Productivity***

Year	1999	2002	2005	2008	2011	2014
Node	180 nm	130 nm	100 nm	70 nm	50 nm	35 nm
% Area New Logic	64%	32%	16%	8%	4%	2%
% Area Reused Logic	16%	16%	13%	9%	6%	4%
% Area Memory	20%	52%	71%	83%	90%	94%
Transistor Logic Density (Mtrans/cm ²)	20	54	133	328	811	2000
New Logic Productivity (Mtrans/PY)	1.4	2.1	2.9	4.2	6.0	8.6
Reused Logic Productivity (Mtrans/PY)	2.9	4.1	5.9	8.4	12.0	17.1
Target Design Resource (PY)	10.0	10.5	10.1	9.9	9.7	9.6



** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.