International Technology Roadmap for Semiconductors

2000 Update

Process Integration, Devices, and Structures

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PROCESS INTEGRATION, DEVICES, & STRUCTURES

SUMMARY

Since the publication of the 1999 ITRS, it has become clear that some of the forecast trends were too conservative. In particular, both the MPU transistor gate length scaling and the technology node timing keyed mainly to the DRAM half pitch are proceeding faster than predicted. Also, the ASIC gate length scaling is no longer trailing the MPU scaling. In response, the PIDS TWG has accelerated the scaling of MPU transistor gate length and associated specifications in the 2000 Roadmap update and has set the ASIC gate length equal to the MPU gate length at all nodes. The changes are in Table 28a, Memory and Logic Technology Requirements—Near Term. In the table, for each year through 2001, the MPU gate length is moved forward by one year in the 2000 update compared to the 1999 ITRS, but the gate lengths are left unchanged from 2002 on. Other key specifications such as equivalent T_{ox}, V_{dd}, maximum I_{off}, etc., are also moved forward by one year, following the gate length. The acceleration is halted with the year 2002 because the TWG is concerned about the "red brick wall" in equivalent T_{ox} that appears in 2005 in the 1999 ITRS. The equivalent T_{ox} is small enough in 2005 to perhaps require high K material for the gate dielectric to keep the gate leakage within acceptable limits, but the industry has no solution in hand. Furthermore, prospects of such a solution by 2005 are highly uncertain. Moving the gate length and thus the equivalent T_{ox} forward by one year for the 2002 node and beyond could result in requiring high K gate dielectric earlier than 2005, which the TWG found unrealistic. The issue of accelerating the gate length and other parameters for 2002 and beyond requires careful analysis of scaling issues.

Other changes are relatively minor, to correct minor errors, update several values in the tables, and clarify explanations in the notes. In Table 28, the changes include an improved definition of the gate delay metric in Rows 9 and 13, making the S/D extension junction depth values and colors in Row 16 the same as those in the Front End Processing Table 34, and recognition of special difficulty, starting in 2002, in meeting the gate leakage requirements for low power transistors (see Note 11). In Table 29, many of the values have been updated.

Currently, there is not a consensus amongst the TWGs and the IRC on the acceleration in scaling trends for DRAM half pitch and MPU/ASIC gate length, especially in 2002 and beyond. It is vitally important to come to consensus early in 2001 regarding the appropriate scaling trend to use. A major challenge for the PIDS TWG will be to then analyze in detail the resulting impact on device and DRAM scaling and characteristics, including especially the accelerated development and integration of high K gate dielectric. Another key challenge will be to work with the FEP TWG to add flash and FERAM characteristics to the tables, and to expand the logic low power requirements. Other key challenges will be to work with the Design TWG to resolve linked device, circuit, and system issues, such as the impact of gate leakage on logic circuitry, the impact of V_{dd} and I_{off} specifications on circuit and system power, etc. Finally, updating and improving the novel devices table will be a major focus.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

2000 UPDATE TABLES

MEMORY AND LOGIC

*Table 28a Memory and Logic Technology Requirements—Near Term***

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
1	DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	
2	MPU/ASIC Physical Gate Length	120	100	90	85-90	80	70	65	
3	MPU / ASIC ½pitch (nm)	230	210	180	160	145	130	115	
4									
5	Minimum logic V_{dd} (V) (desktop)	1.5–1.8	1.2-1.5	1.2–1.5	1.2–1.5	1.2–1.5	0.9–1.2	0.9–1.2	
6	T_{ox} equivalent (nm)	1.9–2.5	1.5-1.9	1.5–1.9	1.5–1.9	1.5–1.9	1.2–1.5	1.0–1.5	M GATE
7	Nominal I_{on} at 25 °C (μA/μm) [NMOS/PMOS] high-performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	M GATE
8	Maximum I_{off} at 25 °C (nA/μm) (For minimum L device) high performance	7	8	10	10	13	16	20	M GATE
9	Gate delay metric CV/I (ps) high-performance	12.5	11.4	10.3	9.7	9.1	8.1	7.5	
10	Percent static power reduction necessary due to innovative circuit/system design	0	48	55	55	71	77	81	M GATE M & A ½
11	Nominal I_{on} at 25 °C (μA/μm) [NMOS/PMOS] low power	490/230	490/230	490/230	490/230	490/230	490/230	490/230	A GATE
12	Maximum I_{off} at 25 °C (pA/μm) (For minimum L device) low power	7	8	10	10	13	16	20	A GATE
13	Gate delay metric CV/I (ps) low power	20.9	17.6	15.9	15.0	14.1	12.9	11.6	
14	Percent static power reduction necessary due to innovative circuit/system design	0	55	65	65	80	85	88	A GATE M & A ½
15	V_t 3σ variation (±mV) (for nominal L_g device)	50	42	42	42	42	33	33	M GATE
16	S/D extension junction depth, nominal (nm)	36–60	30–50	25–43	25–43	24–40	20-35	20-33	M GATE

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

*Table 28a Memory and Logic Technology Requirements—Near Term (continued)***

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
1	DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	
2	MPU/**ASIC** Physical Gate Length	**120**	**100**	**90**	85-90	80	70	65	
3	MPU / ASIC ½pitch (nm)	230	210	180	160	145	130	115	
17	Gate sheet resistance (Ω/sq) at minimum dimension	4–6	4–6	4–6	4–6	4–6	4–6	4–6	M Gate
18	Interconnect levels	6–7	6–7	7	7–8	8	8	8–9	M & A ½
19	Short wire **minimum** pitch **(nm)**	**360-460**	**330-420**	**300-360**	260-320	240-290	220–260	200–230	M & A ½, **D ½**
20	Maximum wire length **for local levels,** Lm (µm)	2243	2036	1828	1621	1468	1315	1162	M & A ½
21	DRAM cell size (µm²)	0.26	0.22	0.18	0.10	0.08	0.065	0.044	D ½
22	DRAM cell dielectric T_{ox} equivalent (nm)	3	2.40	1.80	0.95	0.80	0.65	0.45	
23	**DRAM** retention time (ms)	250	250	250	250	250	250	250–500	
24	DRAM soft error rate (fits)	1000	1000	1000	1000	1000	1000	1000	
25	Nonvolatile data retention **(Years)**	10	10	10	10	10	10	10	
26	NOR cell size (µm²)	0.34	0.29	0.24	0.17	0.15	0.13	0.1	M & A ½
27	+/- V_{pp} **(V)**	8–10	8–10	8–9.5	8–9.5	8–9.5	7–9	7–9	
28	Tunnel oxide (nm)	8–10	8–10	8–9.5	8–9.5	8–9.5	8–9	8–9	
29	NVM endurance (erase/write cycles)	100K	100K	100K	100K	100K	100K	100K	
30	ESD protection voltage (V/µm)	7.5	7.5	10.5	10.5	10.5	12	12	
31	(V/µm²)	2.5	2.5	3.0	3.0	3.0	3.5–4.0	3.5–4.0	

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

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2000 Update										
Year of Production Technology Node (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Year of Production Technology Node **(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

*Table 28b Memory and Logic Technology Requirements—Long Term***

	Year *Technology Node*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	*DRIVER*
[1]	*DRAM ½ Pitch (nm)*	*70*	*50*	*35*	
[2]	*MPU Gate Length (nm)*	*45*	*32*	*22*	
[3]	*MPU / ASIC ½ Pitch (nm)*	*80*	*55*	*40*	
[4]	*ASIC Gate Length (nm)*	*70*	*50*	*35*	
[5]	Minimum logic V_{dd} (V) (desktop)	0.6–0.9	0.5–0.6	0.3–0.6	*M Gate*
[6]	T_{ox} equivalent (nm)	0.8–1.2	0.6–0.8	0.5–0.6	*M Gate*
[7]	Nominal I_{on} at 25 °C (μA/μm) [NMOS/PMOS] high performance	750/350	750/350	750/350	*M Gate*
[8]	Maximum I_{off} at 25 °C (nA/μm) (For minimum L device) high-performance	40	80	160	*M Gate*
[9]	Gate delay metric CV/I (ps) high-performance	4.9	3.4	3.0	
[10]	Percent static power reduction necessary due to innovative circuit/system design	91	97	98	*M Gate* *M & A ½*
[11]	Nominal I_{on} at 25 °C (μA/μm) [NMOS/PMOS] low power	490/230	490/230	490/230	*A Gate*
[12]	Maximum I_{off} at 25 °C (pA/μm) (For minimum L device) low power	40	80	160	*A Gate*
[13]	Gate delay metric CV/I (ps) low power	7.4	5.7	2.8	
[14]	Percent static power reduction necessary due to innovative circuit/system design	95	98	99	*A Gate* *M & A ½*
[15]	V_T 3σ variation (±mV) **(for nominal L_g device)**	25	17	17	*M Gate*
[16]	S/D extension junction depth, nominal **(nm)**	***16-26***	***11-19***	***8-13***	
[17]	Gate sheet resistance (Ω/sq) at minimum dimension	4–6	4–6	4–6	*M Gate*

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

*Table 28b Memory and Logic Technology Requirements—Long Term (continued)***

	Year Technology Node	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
[1]	DRAM ½ Pitch (nm)	70	50	35	
[2]	MPU Gate Length (nm)	45	32	22	
[3]	MPU / ASIC ½ Pitch (nm)	80	55	40	
[4]	ASIC Gate Length (nm)	70	50	35	
[18]	Interconnect levels	9	9–10	10	M & A ½
[19]	Short wire **minimum** pitch (µm)	140-160	100-110	70-80	M & A ½, **D ½**
[20]	Maximum wire length **for local levels,** Lm (µm)	697	325	201	M & A ½
[21]	DRAM cell size (μm^2)	0.018	0.0075	0.0031	D ½
[22]	Cell dielectric T_{ox} equivalent (nm)	0.15	0.06	0.043	
[23]	**DRAM retention time** (ms)	250–500	250–500	250–500	
[24]	Soft error rate (fits)	1000	1000	1000	
[25]	Nonvolatile data retention **(Years)**	10	10	0.1–10	
[26]	NOR cell size (μm^2)	0.05	0.025	0.012	M & A ½
[27]	+/- V_{pp} **(V)**	7–8.5	6.5–8.5		
[28]	Tunnel oxide (nm)	7.5–8.5	2–8	2–7	
[29]	NVM endurance (erase/write cycles)	100K	0.1–1M	0.1–10M	
[30]	ESD protection voltage (V/µm)	13.5	15	17.5	
[31]	($V/\mu m^2$)	4.5–5.0	5.5–6.0	7.5–10	

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

Notes for Table 28a and b Memory and Logic Requirements

General Notes:

[A] *The power supply voltage control is ±10%.*

[B] *Control of L_{gate} is ±10% and ±20% for L_{eff}*

[C] *The total series resistance of the S/D is expected to be <10% of the channel "ON" resistance, $R_{on}=V_{dd}/I_{on}D$. Flash products will not make use of a technology node at the time it is introduced for microprocessor or DRAM usage.*

Explanatory Notes for each row of Table 28a and b:

[1] ***These DRAM half pitch numbers are unchanged from the 1999 ITRS. However, developments since the publication of the 1999 ITRS strongly suggest that the scaling trend here is too conservative. A proposal has been made to accelerate this trend (see ORTC tables), and this proposal will be carefully evaluated and its impact analyzed in preparing the 2001 ITRS.***

[2] ***This is the final, as-etched length at the bottom of the gate electrode. These numbers have been changed from those in the 1999 ITRS because developments since the publication of that document strongly suggest that scaling is proceeding faster than expected. Furthermore, the ASIC gate length scaling no longer trails the MPU scaling, so the ASIC gate length has been set equal to the MPU gate length. In this updated table, for each year through 2001 the gate length value is moved to the left by one year (i.e., one year earlier) compared to the 1999 ITRS, but the gate length values are left unchanged from 2002 on. Other key specifications such as equivalent T_{ox}, V_{dd}, maximum I_{off}, nominal I_{on}, etc., are linked to the gate length, and hence are also moved to the left by one year through 2001 and left unchanged for 2002 and beyond.***

The accelerated scaling is not extended beyond 2001 mainly because of concerns about the equivalent T_{ox} specification. In the 1999 ITRS, the equivalent T_{ox} is small enough in 2005 to perhaps require high K material for the gate dielectric in order to keep the gate leakage within acceptable limits. However, the industry has no solution in hand for such a high K gate dielectric, and prospects of implementing such a solution in production by 2005 are highly uncertain. Accelerated scaling of the gate length and thus the equivalent T_{ox} for 2002 and beyond could result in requiring high K gate dielectric earlier than 2005, which is unrealistic. There are proposals (see the ORTC tables) for accelerated scaling of the gate length in 2002 and beyond, and these will be evaluated in preparing the 2001 ITRS. Such accelerated scaling will require re-evaluation of the equivalent T_{ox} scaling and resolution of difficult overall transistor scaling, CD control, and other issues

[3] *From ORTC table*

[4] ***Row 4 was for the ASIC Gate Length in the 1999 ITRS. However, as explained in Note 2 above, the ASIC gate length scaling has matched the MPU gate length scaling, so ASIC gate length has been set equal to the MPU gate length in the 2000 update. Hence, for the 2000 ITRS, Row 2 covers both MPU and ASIC gate length, and Row 4 is unnecessary.***

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

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2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

[5] *Power supply voltage is based on controlling the active power dissipation (see linked spreadsheet) and keeping the field in the gate dielectric at reasonable levels per reliability concerns. Generally, the higher values in the range will be used for high-performance applications, while the lower values in the range will be used for low-power applications.*

[6] *This is the equivalent effective physical SiO_2 thickness. (Note that the electrically determined oxide thickness from C-V measurements would be larger than the thickness in this line because of polysilicon depletion and quantum effects.)* ***The values here are the same as those in Table 34 in the Front End Processes chapter.*** *Generally, as with V_{dd}, the higher values in the range will be used for high-performance applications, while the lower values in the range will be used for low-power applications. For the 180 through the 110 nm nodes, the range of equivalent T_{ox} is chosen to keep $V_{dd}/T_{ox} \leq 8$ MV/cm because of oxide reliability concerns, where V_{dd}/T_{ox} is a metric for the electric field in the oxide. At the 100 nm technology node, there is a distinct likelihood that high κ materials other than SiO_2 or oxynitride will be used for the gate dielectric. For such materials, the gate leakage current is much smaller than for oxide dielectric with the same equivalent Tox, allowing smaller Tox and hence higher I_{on} for the high κ case. Also, the $V_{dd}/T_{ox} \leq 8$ MV/cm requirement may not hold for the high κ materials, and hence from a reliability point of view, T_{ox} can be scaled further for these materials. Thus, at the 100 nm node, the wide range of 1.0–1.5 nm for equivalent T_{ox} comprehends the uncertainty of what dielectric material will be used, with the high end of the range appropriate for SiO_2 or oxynitride and the very bottom end of the range appropriate for high κ materials. Beyond the 100 node, the use of high κ material for the gate dielectric becomes much more likely, and the $V_{dd}/T_{ox} \leq 8$ MV/cm requirement is no longer followed*

[7] *The device I_{on} value is expected to remain relatively constant for succeeding technology generations.* ***The white, yellow, and red coloring here follows that of T_{ox} in Line 6.***

[8] *The device I_{off} value is projected to increase with successive technology generations to maintain I_{on} constant per Line 7. I_{off} is measured with $V_s=V_g=V_{substrate}=0$ and $V_d=V_{dd}$. I_{off} is the difference between the drain current and the gate (leakage) current (I_{off} is the sum of the subthreshold current [the current in the source lead] and the junction leakage current [the current in the substrate lead]). The requirements on the gate leakage current are listed in the Front End Processes (FEP) chapter in Table 34.* ***This row is colored white throughout because through adjustment of the threshold voltage implant (and perhaps use of other techniques such as optimized halo implants), meeting the I_{off} specification should be achievable. What will be difficult is to simultaneously meet the I_{off} requirement and other key device requirements, especially for I_{on}, at the later technology nodes. The coloring of Row 7 captures this difficulty for I_{on}.***

[9] ***The gate delay metric for high-performance devices is calculated using the approach in Taur and Ning, <u>Fundamentals of Modern VLSI Devices</u>, Cambridge University Press, 1998, pp. 228 - 230. We assume a CMOS inverter with Wp = (Ion,n/Ion,p) * Wn = (750/350) * Wn, where Wn and Wp are the widths of, respectively, the NMOS and PMOS transistors, and the inverter is driven by an ideal square wave at its input. Also, the inverter's load is an identical inverter. Under those circumstances, the CV/I gate delay metric equals the switching delay, τ, in Taur and Ning, where τ = (τn + τp)/2, and τn and τp are defined, respectively, in Equations 5.3 and 5.4 in Taur and Ning. The highest values of V_{dd} from Row 5 are used in this analysis, along with the largest T_{ox} equivalent values from Row 6. It is assumed that the channel width scales with the channel length. The MPU gate length is used for L. Since the gate delay metric is only a calculated number using transistor characteristics such as T_{ox} V_{dd}, etc., the coloring here is white.***

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YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

[10] *For each technology node, maximum system-imposed limits for total chip leakage current, $I_{L,SYS}$, were estimated by assuming a static power dissipation limit of 10% of the maximum heat-sink limit, and dividing this static power dissipation by V_{dd}. Given the projected device I_{off} value from Line 8, the total projected static leakage current for the chip was calculated based on the total number of transistors and an assumed W/L ratio of 3. This projected chip static leakage current was increased by a factor of 100 to account for the leakage current increase due to device self heating (T=100°C). If this projected T=100°C chip static leakage current value is greater than $I_{L,SYS}$, then the excess percentage of static power dissipation is listed in Line 9. This excess must be eliminated through innovative circuit or system design techniques such as using dynamic or multi-V_t techniques to reduce the effective I_{off} of the chip or by turning off sections of the chip temporarily. System values of the heat-sink dissipation limit, the power-supply voltage, chip size and transistor density were obtained from the ORTC tables.*

[11] *For successive technology generations, the device I_{on} value is expected to remain relatively constant. The low-power device performance is a calculated percentage of the high-performance I_{on} value; this calculated value takes into account the loss in current drive due to the higher required threshold voltage necessary in order to satisfy more stringent I_{off} requirements.* ***The color is yellow at the 130 nm node (2002) because of difficulty in meeting the gate leakage specification of ≤10 pA/μm at 100 °C, and the color is red for 2004 and beyond because of the greater difficulty of meeting the gate leakage specifications with the increasingly thin equivalent T_{ox} values at those nodes.***

[12] *The device I_{off} value is set to three orders of magnitude less than the I_{off} for the high-performance chips (Line 8), and is similarly projected to increase with succeeding technology generations. I_{off} is the difference between the drain current and the gate (leakage) current (I_{off} is the sum of the subthreshold current [the current in the source lead] and the junction leakage current [the current in the substrate lead]). The requirements on the gate leakage current are listed in the Front End Processes chapter in Table 34.*

[13] ***The gate delay metric for the low-power devices is calculated using the approach in Yuan and Taur, similarly to calculating the gate delay metric for high-performance devices (see Note 9 above). The only difference from the high-performance case is that the smallest values of V_{dd} from Row 5 and the smallest T_{ox} equivalent values from Row 6 are used in the analysis, and the I_{on} values are those for low-power devices.***

[14] *For each technology node, maximum system-imposed limits for total chip leakage current, $I_{L,SYS}$, were estimated by assuming a static power dissipation limit of 10% of the maximum chip power dissipation, and dividing this static power dissipation by V_{dd}. A reasonable value for the maximum dissipation for high density, battery-operated chips is 100 μW, in order to preserve battery life. Given the projected device I_{off} value from Line 11, the total projected static leakage current for the chip was calculated based on the total number of transistors and an assumed W/L ratio of 3. If this projected chip static leakage current value is greater than $I_{L,SYS}$, then the excess percentage of static power dissipation is listed in Line 12. This excess must be eliminated through innovative circuit or system design techniques such as using dynamic or multi-V_t techniques to reduce the effective I_{off} of the chip or by turning off sections of the chip temporarily.*

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

[15] *The V_t 3-sigma variation was scaled proportionately with the reduction in the midrange power supply voltage.* **The V_t 3-sigma variation here is the total statistical variation in V_t, including the effects of statistical variation in T_{ox}, L_g, implant dose and energy, etc.**

[16] *A range of junction depths can be used depending on the drain and channel engineering used (such as pocket implants versus shallow drain extensions).* **The values and the white, yellow, and red coloring here are the same as those in Table 34 in the Front End Processes chapter.**

[17] *Difficult to obtain gate sheet resistance targets with silicide at 70 nm and beyond.*

[18] *The number of interconnect levels is driven by high-performance microprocessor.*

[19] *The short wire pitch is equal to two times the half pitch.*

[20] *For the metal layers with the smallest pitch, this is the calculated value of the maximum wire length for the propagation delay to be 0.9*$f_{max, local}$, where $f_{max, local}$ is the maximum local frequency from the ORTC tables. The gates are three-input NAND gates, with a Wn/L ratio of 5. (The formula used in calculating the delay as a function of maximum wire length is in P.D. Fisher, et al.[6]) Also refer to the linked spreadsheet.*

[21] *The cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Processes chapter Table 34b. The capacity and chip size numbers used by FEP are from the Overall Roadmap Technology Characteristics (ORTC) Tables 1a and 1b, and reflect the "generation at introduction" option. (This is for the DRAM chip that is just being introduced and sampled, having the highest DRAM capacity and most aggressive but still quite large chip size. Note that the "Generation at production" option in the ORTC tables has one quarter the DRAM capacity of the generation at introduction option, and correspondingly smaller chip size that allows the chip price to be affordable.) Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled very aggressively. The difficulty will lie in reducing the value of the cell size factor, a, where a = cell size/F2 and F is the DRAM half pitch. The required values for a are 8 for the 180 nm node, 6 for the 130 nm node, and 4.4 for the 100 nm node. a = 8 is probably achievable with current techniques, but a =6 will require innovative solutions, as indicated by the yellow coloring of the 130 nm node for this line, while a=4.4 has no known solution, as indicated by the red coloring of the 100 nm node and beyond.*

[6] P. D. Fisher, et al., "The Test of Time," *IEEE Circuits and Devices Magazine*, vol. 14, pp. 37–44 (March 1998).

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

[22] *Cell dielectric T_{ox} equivalent thickness is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Processes chapter, Table 34b. The capacity and chip size numbers used by FEP are from the Overall Roadmap Technology Characteristics (ORTC) Tables 1a and 1b, and reflect the "generation at introduction" option. (This is for the DRAM chip that is just being introduced and sampled, having the highest DRAM capacity and most aggressive but still quite large chip size. Note that the "generation at production" option in the ORTC tables has one quarter the DRAM capacity of the Generation at introduction option, and correspondingly smaller chip size that allows the chip price to be affordable.) Since the FEP DRAM capacity and chip size numbers are quite aggressive, the equivalent T_{ox} must also be scaled very aggressively. For the 180 nm–150 nm nodes, the dielectric is based on ONO/Ta_2O_5. For the 130 nm node and beyond, breakthroughs are needed to utilize MIM structures and eventually BST, while for the 70 nm node and beyond, there are no known solutions. The actual T_{ox} equivalent requirement for each node depends on factors such as area enhancement (by height and 3D structures), film leakage, and contact formation. Trench capacitors may have different requirements for the cell dielectric material, but the trends should be valid..*

[23] *Retention time is the minimum time without refreshing a row that the data from memory is still sensed correctly at 85°C. This is the measure of the combined interaction of device leakage, signal strength, and the sense amplifier circuit's sensitivity. This requirement can vary with operating frequency and temperature, and also depending on the application specifics.*

[24] *Soft error: This is a typical FIT rate and can vary with cycle time and other quality/reliability testing conditions.*

[25] *Retention requirements will remain at ten years in the near term, but future alternative technologies will exploit retention-endurance tradeoffs.*

[26] *The need for high electric fields will complicate scaling and eventually force use of alternative NVM technology.*

[27] *The meaning of V_{pp} has become uncertain because it is no longer an external supply. In this table it is intended to indicate the highest voltage relative to ground seen in the cell array.*

[28] *Tunnel oxides must be thin enough to allow ease of program/erase, but thick enough to assure retention. Scaling difficulties will force consideration of alternative cell structures.*

[29] *Endurance of 100K cycles is a minimum need, and in emerging nodes the possibility of higher endurance and lower retention will be explored.*

[30] *ESD V/µm in terms of NMOS capability per micron width**, based on the Human Body Model**. Particularly critical in NMOS ESD circuits and self-protected circuits.*

[31] *ESD V/μm^2 in terms of protection circuit effectiveness per unit area of the protection circuit including guard ring**, based on the Human Body Model.***

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

ANALOG, MIXED-SIGNAL, AND RF

*Table 29a Analog, Mixed-signal, and RF Technology Requirements—Near Term***

			1999	2000	2001	2002	2003	2004	2005	DRIVER
[1]	YEAR TECHNOLOGY NODE		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
	DRAM ½ Pitch (nm)		180	165	150	130	120	110	100	D
	MPU Gate Length (nm)		140	120	100	85	80	70	65	M Gate
	MPU/ASIC ½ Pitch (nm)		230	210	180	160	145	130	115	M & A
	ASIC Gate Length (nm)		180	165	150	130	120	110	100	A Gate
[2]	Minimum Digital Supply Voltage (V)		1.8–1.5		1.5–1.2			1.2–0.9		M Gate
[3]	Minimum Analog Supply Voltage (V)		3.3–2.5	**3.3**–1.8			2.5–1.8			
[4]	RF Frequency (GHz)		0.9–2.5	0.9–10						
[5]	Analog Frequency (GHz)		<0.1	0.1–5						
[6]	RF Transistor	Current (μA)	100	100	100	100	75	75	75	M Gate
[7]		f_{max} (GHz)	25	28	32	35	40	45	50	
[8]		f_{τ} (GHz)	20	20	25	30	30	35	40	
[9]		Noise figure (dB)	1.5	1.5	1.5	1.5	1.2	1.2	1.2	
[10]		1/f Noise (V^2-μm^2)	1×10^{-11}	1×10^{-11}	1×10^{-11}	5×10^{-12}	5×10^{-12}	5×10^{-12}	1×10^{-10}	
[11]	Analog	Current (μA)	75	70	65	60	55	50	50	
[12]		1/f Noise (V^2-μm^2)	1×10^{-11}	1×10^{-11}	1×10^{-11}	5×10^{-12}	5×10^{-12}	5×10^{-12}	2×10^{-10}	
[13]		Gate oxide leakage (A/cm^2)	–	–	–	–	–	–	1×10^{-10}	
[14]		Current matching (Δ% ±3σ)	≤1	≤1	≤1	≤1	≤1	≤1	≤1	
[15]	RF Coupling	Density ($fF/\mu m^2$)	1	1.2	1.4	1.5	1.7	1.9	2	
[16]		Q	≥15	≥18	≥22	≥25	≥27	≥29	≥30	
[17]	Filter	Density ($fF/\mu m^2$)	2.5	2.8	3.2	3.5	3.7	3.8	4	
[18]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	
[19]	RF Bypass	Density ($fF/\mu m^2$)	5	6	7	7.5	8	9	10	
[20]		Linearity (ppm/V)	≤1000	≤1000	≤1000	≤1000	≤1000	≤1000	≤1000	
[21]		Q	≥15	≥18	≥22	≥25	≥27	≥29	≥30	

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

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2000 Update										
Year of Production Technology Node (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Year of Production Technology Node (Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

*Table 29a Analog, Mixed-signal, and RF Technology Requirements—Near Term (continued)***

[1]	Year Technology Node		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
	DRAM ½ Pitch (nm)		180	165	150	130	120	110	100	D
	MPU Gate Length (nm)		140	120	100	85	80	70	65	M Gate
	MPU/ASIC ½ Pitch (nm)		230	210	180	160	145	130	115	M & A
	ASIC Gate Length (nm)		180	165	150	130	120	110	100	A Gate
[22]	Analog	Density ($fF/\mu m^2$)	1	1	1	1.5	1.5	1.5	2	
[23]		Linearity (ppm/V)	≤100	≤100	≤100	≤100	≤100	≤100	≤100	
[24]		Leakage **(pA/pF-V)**	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	
[25]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	
[26]	RF Resonator	Q	<50	<50	<50	50–1000				
[27]	Analog	Matching (Δ% ±3σ)	≤1	≤1	≤1	≤0.1	≤0.1	≤0.1	≤0.1	
[28]		1/f Noise (A^2-μm^2)	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	
[29]		TC (ppm/°C)	≤100	≤100	≤100	≤10	≤10	≤10	≤10	
[30]	Inductor	Q	≥15	≥15	≥25	≥25	≥25	≥25	≥30	
[31]	Signal Isolation	S_{21} (dB)	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-120	
[32]	Benchmark	Gain (dB)	≥20	≥20	≥20	≥20	≥20	≥20	≥20	
[33]		IIP3 (dBm)	-4	-4	-4	-3	-3	-3	-2.5	
[34]		Noise figure (dB)	1.5	1.5	1.5	1.3	1.3	1.3	1.2	
[35]		Noise (dB)	4	4	4	3.5	3.5	3.5	3	
[36]		Resolution (Bits)	8–14			8–14				

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

*Table 29b Analog, Mixed-signal, and RF Technology Requirements—Long Term***

[1]	YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
	DRAM ½ Pitch (nm)	70	50	35	D
	MPU Gate Length (nm)	45	32	22	M Gate
	MPU / ASIC ½ Pitch (nm)	80	55	40	M & A
	ASIC Gate Length (nm)	70	50	35	A Gate
[2]	Minimum Digital Supply Voltage (V)	0.9–0.6	0.6–0.5	0.5–0.3	M Gate
[3]	Minimum Analog Supply Voltage (V)	1.8–1.5		1.5	
[4]	RF Frequency (GHz)	0.9–10	0.9–100		
[5]	Analog Frequency (GHz)	0.1–5	0.1–10		
[6]	RF Transistor Current (μA)	50	50	50	
[7]	f_{max} (GHz)	60	150	175	
[8]	f_{τ} (GHz)	50	120	140	M Gate
[9]	Noise figure (dB)	≤1	≤1	≤1	
[10]	1/f Noise (V^2-μm^2)	5×10^{-11}	2×10^{-11}	1×10^{-11}	
[11]	Analog Current (μA)	40	30	20	
[12]	1/f Noise (V^2-μm^2)	1×10^{-10}	1×10^{-10}	5×10^{-11}	
[13]	Gate oxide leakage (A/cm^2)	1×10^{-08}	1×10^{-08}	1×10^{-05}	
[14]	Current matching (Δ% ±3σ)	≤1	≤1	≤1	
[15]	RF Coupling Density (fF/μm^2)	3	4	6	
[16]	Q	≥35	≥40	≥40	
[17]	Filter Density (fF/μm^2)	5	7	10	
[18]	Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	
[19]	RF Bypass Density (fF/μm^2)	15	20	30	
[20]	Linearity (ppm/V)	≤1000	≤1000	≤1000	
[21]	Q	≥35	≥40	≥40	

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* ***(1999 ITRS)***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

*Table 29b Analog, Mixed-signal, and RF Technology Requirements—Long Term (continued)***

[1]	*Year* *Technology Node*		*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	*Driver*
	DRAM ½ Pitch (nm)		*70*	*50*	*35*	*D*
	MPU Gate Length (nm)		*45*	*32*	*22*	*M Gate*
	MPU / ASIC ½ Pitch (nm)		*80*	*55*	*40*	*M & A*
	ASIC Gate Length (nm)		*70*	*50*	*35*	*A Gate*
[22]	*Analog*	Density (fF/μm^2)	**3**	**4**	**6**	
[23]		Linearity (ppm/V)	**≤100**	**≤50**	**≤50**	
[24]		Leakage ***(pA/pF-V)***	**≤0.001**	**≤0.001**	**≤0.001**	
[25]		Matching (Δ% ±3σ)	**≤0.1**	**≤0.1**	**≤0.1**	
[26]	*RF*	Q	**50–1000**		**≥1000**	
[27]	*Analog*	Matching (Δ% ±3σ)	**≤0.1**	**≤0.1**	**≤0.01**	
[28]		1/f noise (A^2-μm^2)	**1×10^{-18}**	**1×10^{-18}**	**1×10^{-18}**	
[29]		TC (ppm/°C)	**≤10**	**≤10**	**≤1**	
[30]	*Inductor*	Q	**≥50**	**≥75**	**≥75**	
[31]	*Signal Isolation*	S_{21} (dB)	**≤-120**	**≤-120**	**≤-120**	
[32]	*Benchmark*	Gain (dB)	**≥20**	**≥20**	**≥20**	
[33]		IIP3 (dBm)	**-1.5**	**-1**	**-1**	
[34]		Noise figure (dB)	**1.0**	**1.0**	**1.0**	
[35]		Noise (dB)	**2.5**	**2**	**2**	
[36]		Resolution (Bits)	**8–14**		**≥24**	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 29a and bAnalog, Mixed-signal, and RF Requirements

Explanatory Notes for each row of Tables 29

[1] *Year of first digital product for a given technology generation. Lithographic drivers for key technologies at each node are indicated. Year of first analog, RF, and mixed-signal product at the same technology may lag by one generation.*

[2] *Digital (logic V_{dd}) supply voltage, driven by MPU gate length (M Gate), is repeated here for reference.*

[3] *Analog supply voltage is expected to lag digital by two or more generations. Additional voltage headroom is needed to avoid excessive power dissipation under reduced signal swing conditions. Analog CMOS designs may use thick gate oxide and low V_t techniques. The analog power supply reduction trend may lag digital backward compatibility trend for I/O such that a common thick gate oxide solution is not feasible.*

[4] *RF applications will focus on the 0.9– 2.5 GHz, 5– 6 GHz, 17– 20 GHz, 40– 45 GHz, and 60– 65 GHz frequency spectrums. Design of applications at the lower frequencies will continue throughout the duration of the roadmap (lower frequency bands are not "obsoleted" and will continue to be used). Higher frequency bands will drive performance requirements.*

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YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

[5] *General purpose analog frequency (such as DSP, audio/video, ADC) trend is in parallel with RF. Very clean, jitter-free, clock frequency generation is required. Transistors: It is expected that speed × power characteristics favor use of bipolar for* $\mathbf{W_e}$ < *180 nm. MOS speed × power may be favorable relative to bipolar at* L_{eff} > *180 nm. Bipolar device assumed through 110 nm (see Potential Solutions Figure 14) followed by MOS device.*

[6] *Absolute current (independent of device geometry) at which these key RF transistor parameters are measured.*

[7] *Assumes a "rule of thumb" of approximately 10× the transmit/receive frequency.*

[8] *Assumes that ft generally follows the progression of* f_{max}.

[9] *Measured at the specified current (Row 5) and at the application transmit/receive frequency (Row 4).*

[10] *Bipolar device assumed* ***up to and including the 110 nm node*** *(see Potential Solutions Figure 14) followed by MOS device. Assume SPICE model for MOS device: SVG=Kf/(*C_{ox}^2*×W×L×f). Values scaled assuming* t_{ox}^2 *relationship.1/f spectral density is normalized to active device area=1* μm^2*, frequency=1Hz. RF MOS device assumed to be realized with the thinnest gate oxide and shortest* L_{eff} *available at a given node. For this reason, the minimum MPU gate length (M Gate) is indicated as a driver for this device. Although the effects are acute at baseband, 1/f noise can be "mixed up" to RF if present in RF devices. The effect is prominent in MOS devices due to carrier recombination in traps at the insulator-semiconductor interface (surface effect).*

[11] *Absolute current (independent of device geometry) at which these key analog transistor parameters are measured.*

[12] *Bipolar device assumed* ***upto and including the 110 nm node*** *(see Potential Solutions Figure 14) followed by MOS device. Assume SPICE model for MOS device: SVG=Kf/(*C_{ox}^2*×W×L×f). Values scaled assuming* t_{ox}^2 *relationship. 1/f spectral density is normalized to active device area=1* μm^2*, frequency=1Hz. Analog MOS device assumed to use the thicker or analog gate oxide available at a given node. The effect is prominent in MOS devices due to carrier recombination in traps at the insulator-semiconductor interface (surface effect). Vertical devices (bipolar) or sub-surface devices (JFETs) are superior in this regard.*

[13] ***Bipolar device assumed up to and including the 110 nm node (see Potential Solutions Figure 14) followed by MOS device. Hence, gate oxide leakage has no meaning until the 110 nm node (2004), and the boxes for the previous nodes are left with just a dash in them. For CMOS, analog*** *power supply constrains minimum gate oxide thickness (and therefore leakage).* ***T_{ox}=4 nm (100 nm node)****;* T_{ox}*=3.5 nm (70–50 nm nodes);* T_{ox}*=3 nm (35 nm node).*

[14] *Matching specification assumes "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity are required.*

[14] ***Bipolar device assumed up to and including the 110 nm node (see Potential Solutions Figure 14) followed by MOS device.*** *Matching specification assumes "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity are required.* ***Bipolar values specified for an emitter area of 20µm², CMOS values specified at a gate overdrive,*** ***V_{gs}-V_{th}, of 200mV and an area of 250µm².***

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Year of Production *Technology Node* **(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

[15] *RF coupling capacitors are not expected to drive density. Linearity is not driven by this capacitor.*

[16] *Q is the most important parameter for this type of capacitor. Low series R and low parasitics are key.*

[17] *Analog filter implementations will drive density to 7 fF/μm². As digital filter solutions dominate beyond 2003, bypass capacitor applications will drive density. As digital content increases, chip size decreases, and capacitors occupy a larger percentage of a chip. Choice of implementation is driven by complexity/chip size tradeoff (cost). microelectromechanical systems (MEMS) implementation for filter applications may be favorable at density = 7 fF/μm². Voltage linearity and leakage are not driven by this capacitor.*

[18] *Matching important for this capacitor. Specified at a value of 1 pF.*

[19] *As digital filter solutions dominate beyond 2003, bypass capacitor applications will drive density. High κ dielectrics may be cost-effective as chip size decreases in the 5– 15 year timeframe. Density is driven by low frequency requirements and chip size considerations.*

[20] *Voltage linearity not driven by this capacitor.*

[21] *Q is important for this capacitor to provide bypass response at high frequency. Massively parallel, parasitic implementations are expected to dominate for the next five years.*

[22] *Analog capacitors do not drive density.*

[23] *Voltage linearity is driven by switched capacitor applications. Low series R is key.*

[24] *Leakage is driven by feedback capacitor applications where a long time constant is required. Requirement is relaxed with increasing analog clock frequency. Highest quality dielectric is suggested.*

[25] *Matching is key for analog capacitors. Specified at a value of 1 pF.*

[26] *Q is important for this resonator. Low RF parasitic structures such as MEMS polysilicon structures are long-term solutions (see Potential Solutions Figure 14).*

[27] *Matching is important for the analog resistor. Careful layout and photolithographic uniformity are required. Minimum dimensions assumed to be larger than minimum technology dimensions.* ***Specified at a value of 1 MΩ.***

[28] *1/f noise requirement is most important for the analog resistor. It is assumed that low 1/f solutions other than polysilicon coincide with high Q RF resistor solutions.* ***1/f spectral density is normalized to resistor area=1 μm², frequency=1 Hz.***

[29] *Temperature coefficient is important for the analog resistor. Low TC films or TC canceling techniques may be utilized*

[30] *Q is most important for the inductor. Low series R implementations such as thick copper is assumed for the next five years. CMOS trend toward increasing substrate doping conflicts with inductor integration. Solutions that mitigate the CMOS conflict and maintain Q are assumed.*

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2000 Update										
Year of Production *Technology Node* **(1999 ITRS)**	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* ***(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)***	*1999* *180 nm*	*2000*	*2001* ***130 nm***	*2002*	*2003*	*2004* ***90nm***	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

[30] Q is most important for the inductor. Low series R implementations such as thick copper is assumed for the next five years. CMOS trend toward increasing substrate doping conflicts with inductor integration. Solutions that mitigate the CMOS conflict and maintain Q are assumed. ***Specified at L = 1 nH and f = 1 GHz.***

[31] Signal isolation is best defined as the transmission efficiency (S21 in dB) between a noise source and a noise sensor. Transient sensitivity (in V peak-to-peak) is also an important measure of signal isolation but is not quantified due to its dependence on layout and package. System partitioning, metal interconnect scheme, substrate resistivity, and package design have significant impact on the signal isolation performance. Final result is dependent on application and design tradeoffs.

[32] Gain for low-noise amplifier and mixer benchmark circuits

[33] IIP3 for low-noise amplifier and mixer benchmark circuits

[34] Noise figure for a low-noise amplifier benchmark circuit

[35] Noise for a mixer benchmark circuit

[36] Resolution for A/D, D/A benchmark circuits required for audio/video applications

Several trends have been identified for analog, RF and mixed-signal requirements that will lead to higher levels of integration with logic: raw speed of the logic process will enable more signal processing in the digital realm and the implementation of some RF functions; use of dual-gate oxides for higher voltage logic I/O's will support analog requirements for signal headroom; continued focus on 1/f noise, capacitor density and component matching will be required for power and area efficient design.

Modularity of process features will be desirable in order to adapt the technology to specific SoC architectures. Optimization of the logic process to meet analog transistor specifications may add process complexity, but will be required to achieve mixed-signal integration goals. CMOS will continue to be the technology of choice except for applications where Si or SiGe BiCMOS offers a clear performance or area advantage in high-speed circuits.

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RELIABILITY

Table 30a Reliability Technology Requirements—Near Term

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Customer Reliability Expectations (at 85° C Junction Temperature)								
[1]	Early failures (ppm) (First 4000 operating hours)	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
[2]	Long term reliability (5–10 Years) (FITs = failures in 1E9 hours)	10–100	10–100	10–100	10–100	10–100	10–100	10–100
[3]	Soft error rate (FITs)	1000	1000	1000	1000	1000	1000	1000
[4]	Relative failure rate per transistor (normalized to 180 nm)	1	1	1	.62	.62	.62	.34
[5]	Relative failure rate per m of Interconnect (normalized to 180 nm)	1	1	1	.51	.51	.51	.34
[6]	System-on-a-Chip reliability prediction	Logic and Memory			MicroMachine			Micro Optics
[7]	Failure analysis cycle time (days)	1–12	1–12	1–12	1–10	1–10	1–10	1–10

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Note: Reliability requirement includes chip and package failures. Additional parameters (such as temperature cycling and humidity) need to be specified for package reliability.

Table 30b Reliability Technology Requirements—Long Term

	YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Customer Reliability Expectations (at 85° C Junction Temperature)				
[1]	Early failures (ppm) (First 4000 operating hours)	50–2000	50–2000	50–2000
[2]	Long term reliability (FITs = Failures in 1E9 hours) (5–10 Years)	10–100	10–100	10–100
[3]	Soft error rate (FITs)	1000	1000	1000
[4]	Relative failure rate per transistor (normalized to 180 nm)	.16	.07	.03
[5]	Relative failure rate per m of interconnect (normalized to 180 nm)	.18	.10	
[6]	System-on-a-Chip reliability prediction	Micro Biological		
[7]	Failure analysis cycle time (days)	1–10	1–10	1–10

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 30a and b Reliability Requirements

[1, 2, 3, 5] *Reliability requirements vary with application. For many mainstream customers it will be sufficient to hold current reliability levels steady during this period of rapid technological change. However, other customers would like reliability levels to improve. Degradation of current reliability levels is not acceptable.*

[1] *Early failures are generally associated with defects.*

[3, 4] *Inverse of number of transistors per generation (3) or meters of interconnect per generation (4). For the reliability levels of the chip to remain constant (1,2) the failure rate per transistor or per meter of interconnect must be reduced.*

[6] *Need to develop the capability to predict the reliability of advanced technologies then will be integrated onto advanced Systems-on-a-Chip. Dates when technologies will be inserted are approximate.*

[7] *The time to complete the determination of the cause of a yield, field or design failure.*

2000 UPDATE										
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YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

BEYOND CMOS / NOVEL DEVICES

Non – Bulk CMOS Devices Table

Device	INSERTION NODE (NM)	APPLICATION DRIVER (PERFORMANCE, POWER, COST)	INSERTABILITY (SYSTEM)	INSERTABILITY (INFRASTRUCTURE)	ADVANTAGES	CHALLENGES
SOI (PD)	*180*	*Low Power especially. Performance*	*OK*	*OK*	*Low power, high speed, low voltage operation, reduced SER*	*Cost, Dynamic body charge*
SOI (FD)	*130*	"	"	"	*Low power, high speed, low voltage operation, reduced SER*	*Cost, Control of very thin Si layer*
Multi-Vt Logic MOS	*180*	*Performance*	*OK*	*OK*	*High system speed @ relatively low power*	*Cost*
Multi-value logic	*≤100*	*Cost*	*Very Difficult*	*Difficult*	*Density*	*V t control, speed.*
Dynamic Vt logic (gate tied to body)	*≤100 (0.6V restriction on Vdd drives this choice.)*	"	*". (Note: 0.6V restriction on Vdd is less than ITRS's Vdd for 100 nm node.)*	"	*High speed @ relatively low power*	*Cost, Junction leakage. Restricted to Vdd≤0.6 V. For bulk, isolation is an issue.*
Vertical MOSFET	*≤130 (DRAM)* *≤70 (logic)*	*Performance*	*Issues. (Only one Lg =>no good for analog.)*	*Difficult Issues*	*Litho independence, high Idrive*	*Processing,* *Process integration. Standard CMOS needed on same chip.*
Double Gate SOI	*≤70*	*Performance*	"	*Difficult Issues*	*Improved short channel, high Idrive*	*Cost, how to fabricate self-aligned double gate*
Epi channels, including SiGe	*≤70*	*Performance*	*OK*	*OK*	*High mobilities for electrons and holes*	*Process complexity, novel materials and processes*

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YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

Non-Bulk MOS Technology Descriptions

TECHNOLOGY	DESCRIPTION
SOI (PD)	Partially depleted SOI MOSFETs
SOI (FD)	Fully depleted SOI MOSFETs
Multi-Vt Logic	Multiple threshold voltages provided by a second gate fabricated as a mirror image of the control gate
Multi-Value Logic	Logic gates/primitives providing 3 or more logic states
Dynamic-Vt Logic	Second gate is connected to the body providing high Vt in the off-state and low Vt in the on-state
Vertical MOSFET	MOSFETs fabricated with the source/gate/drain vertically aligned providing for either horizontal or vertical current flow
Double Gate SOI	SOI MOSFETs fabricated with 2 gates providing charge control on the two channel interfaces between the source/drain
Epi Channels	MOSFETs containing group IV alloy (SiGe, SiGeC, etc.) epitaxially grown channels
Delta-Type MOSFET	MOSFET in which the channel has a spiked or delta doping
MEM(D)S	Micro-Electro-Mechanical devices/structures fabricated in silicon (e.g., electrical and optical switches, RF resonators, imagers, etc.)

Novel Logic Devices Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
MEMS	100 (dependent on solving difficult problems, not on 100 nm node CDs)	-Cost, Sys on Chip (RF resonators, imaging, sensors) -ULSI switching (open and close) -Microelectronic chem. Sensors	Difficult issues	Difficult issues	Great SOC flexibility, possible speed, lower power, and low crosstalk (optical interconnect)	Integration of MEMS and Si systems; reliability
Resonant Tunneling IC	≤35	Performance, RF	Difficult issues	Difficult issues	Density, performance, RF	Entirely new IC device
3D Stack Structures	≤35	Cost, power	Issues, especially with interconnect	Difficult issues	Very high density & Short interconnects	Process complexity, Heat dissipation
Organic Transistors (could be on plastic substrate)	≤35	Cost, power	Difficult issues	Difficult issues	Cost, power	Entirely new IC device. Temperature limitations during processing
CHINTS (chan. hot electron injection transistor)	≤35	Performance, power	Difficult issues	Issues	Density, power, performance (multi-value logic)	Entirely new IC device
Carbon Nanotube transistor	≤35	Performance, power	Difficult issues	Difficult issues	Density, power	New device & system

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Novel Logic Device Tables (continued)

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
Single Electron Transfer	*≤35*	*Cost*	*Difficult Issues*	*Difficult Issues*	*Desity*	*New devices & system, Room temp operation questionable, noise (offset charge). Lack of drive current*
Crbon Nanotube Transistor	*≤35*	*Performance, Power*	*Difficult Issues*	*Difficult Issues*	*Desity, Power*	*New Devices & System*

Novel Logic Device Technology Descriptions

Technology	Description
3D Stack Structures	*CMOS gates fabricated with the p-channel MOSFET stacked on top the n-channel MOSFET. Also, ICs fabricated with 2 or more active layers (containing CMOS gates with interconnect layers) stacked Resonant*
Tunnel Diode (RTD) IC	*An IC fabricated solely using resonant tunneling diodes (negative differential resistance diodes whose conduction state depends upon energetic coincidence of an electrode Fermi energy with a quantum state formed between 2 high-energy barrier potentials). The IC may also consist of RTDs combined with CMOS gates.*
Organic Transistors	*Transistors fabricated in polymer materials, perhaps, using plastic substrates*
CHINTS	*Channel hot electron injection transistor - Channel charge density is supplied by the injection of hot electrons from an electrode*
Carbon Nanotube Transistor	*A transistor fabricated using amphoteric carbon nanotube technology*
Single Electron Transistor	*A 3-terminal device based on the Coulomb blockade where the number of electrons on an island or a dot is an integer number controlled by a gate*

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Novel Storage Devices Table

Device	**Insertion Node (nm)**	**Application driver (performance, power, cost)**	**Insertability (system)**	**Insertability (Infrastructure)**	**Advantages**	**Challenges**
FERAM	*180*	*Cost, performance for nonvolatile*	*OK*	*OK*	*high capacitance, nonvolatile, low voltage and power (nonvolatile)*	*Cost, fab., reliability, esp. for highly scaled technology*
Multi level Flash	*180*	*Cost*	*OK*	*OK*	*High density - ==>cost reduction*	*Accurately placing charge on gate, process control, material and reliability*
MRAM	*≤ 100*	*Cost*	*Issues*	*Difficult Issues*	*Density, power, performance, nonvolatility*	*Reliability and integration. Material quality.*
Quantum Dot Memories, including single electron	*<35*	*Cost*	*Difficult Issues*	*Difficult Issues*	*Density, power, , nonvolatile capability*	*New device & system. Room temperature operation difficult.*

Novel Storage Device Technology Descriptions

Technology	*Description*
FERAM	*Ferroelectric RAM*
Multi-Level Flash	*A flash memory cell containing two or more addressable floating gates for charge storage*
MRAM	*An array of ultra-small magnetic sensors with hysteresis forming the bits. The bits are set by a magnetic field generated by 2 crossed conductors carrying a current, with a bit consisting of magnetic thin multilayers exhibiting magnetoresistance, the conductance of which is based on the spin state of the bit*
Quantum Dot	*A memory device in which the storage element consists of 2-terminal Memories quantum dot for storage of multiple or single electrons*

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Novel Systems Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
Cryoelectronics, esp. device optimization for reduced temp. operation	*180 (modest cooling); ≤50 (≤ liq. Nitrogen temp.)*	*Performance*	*OK (180 nm) -Packaging and cooling issues*	*Some Issues*	*Speed, power*	*Cost*
Molecular Electronics	*<35*	*Cost*	*Difficult Issues*	*Difficult Issues*	*Desity*	*Entirely new device, system.*
DNA and Biological Computing	*<35*	*Cost, performance*	*Difficult Issues*	*Difficult Issues*	*Density, power, performance*	*Entirely new device, system.*
Quantum Computing -Spin State Structures - Tunneling Phase Logic	*<35*	*Performance, power*	*Difficult Issues*	*Difficult Issues*	*Density, power, performance*	*Entirely new device, system (NMR readout?)*
Quantum devices: Josephson Junction Tunneling devices	*<35*	*Performance*	*Difficult Issues*	*Difficult Issues*	*Speed and relatively low power*	*Entire new device, system. Room temp. operation.*
All-optical integrated computing and swithing	*<35*	*Performance*	*Difficult Issues*	*Difficult Issues*	*Performance crosstalk reduction*	*Entirely new device and system.*

Novel Systems Technology Descriptions

TECHNOLOGY	DESCRIPTION
Cryoelectronics	*CMOS technology cooled for special, high performance applications*
Molecular Electronics	*Electronic logic and memory elements that function as voltage-operated switches fabricated in single molecules*
DNA & Biological Computing	*DNA Computing: Computational functions performed by a DNA molecule; DNA molecules more likely will guide fabrication of nano-structures via self assembly techniques Biological Computing: Biological cells containing intelligent genes that can add numbers, store bits, keep time and execute programs*
Quantum Computing	*Performance of computational functions using quantum effects realized in systems utilizing the spin states of atomic nuclei or, alternatively, of electrons. Each atom or electron provides two basis functions (spin-up & spin-down) that define the eigenstates of the system; these coupled (or entangled) eigenstates define quantum bits or qubits as a superposition of the eigenstates. Calculations are based on the controlled coherent interaction between the two qubits (entanglement).*
Josephson Junction	*Also known as Rapid Single Flux Quantum Logic (RSFQ) Logic Tunneling Devices where a flux quantum is used as a bit. The switching elements are Josephson Junctions formed of a semiconductor-insulator-semiconductor structure.*

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