

International Technology
Roadmap for
Semiconductors
2000 Update

Assembly and Packaging

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ASSEMBLY AND PACKAGING

2000 UPDATE TABLES

Table 58 Assembly & Packaging Difficult Challenges**

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	SUMMARY OF ISSUES
Improved organic substrates for high I/O area array flip chip	<p>T_g compatible with Pb and Pb free solder processing ϵ_r approaching 2.0</p> <p>Increased wireability at low cost</p> <p>Lower CTE* approaching 6.0 ppm/°C Low moisture absorption High density substrate test</p>
Improved underfills for high I/O area array flip chip Reliability limits of flip chip on organic substrates	<p>Improved manufacturability (fast dispense/cure), better interface adhesion, lower moisture absorption, flow for dense bump pitch</p> <p>Reliability up to 170°C for automotive</p> <p>Comprehensive parametric knowledge of packaging components (chip size, underfill, substrate, heat sink, UBM/bump**)</p>
Coordinated design tools and simulators to address chip, package, and substrate complexity	<p>Physical design</p> <p>Thermal/thermo-mechanical</p> <p>Electrical (power disturbs, EMI†, signal integrity associated w/higher frequency/current, lower voltage, mixed-signal co-design)</p> <p>Commercial EDA‡ supplier support</p>

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Table 58 Assembly & Packaging Difficult Challenges (continued)**

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	SUMMARY OF ISSUES
System reliability impact of Cu/low κ on packaging	Bump and underfill technology to assure low κ dielectric integrity Mechanical strength of dielectrics Interfacial adhesion
Cost effective cooling for cost-performance and high-performance sectors	Meeting 40°C above ambient temperature Localized on-chip power density
<i>Pb, Sb, and Br free packaging materials</i>	<i>Major issue is meeting new requirements including higher reflow temperatures at the present cost goals.</i>
DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Close the gap between the substrate technology and the chip	Low-loss, low ϵ_r materials Cost/unit area constant (cost/layer decreasing) Interconnect density scaled to silicon System level solution that optimizes reliability and cost
“System level” view of integrated chip, package, and substrate needs	<i>System level solution that optimizes reliability and cost</i>
Ultra high frequency design for high density digital and mixed-signal packaging	Efficient design and simulation tools Integrated analog to digital design tools
Manufacturability and reliability of large body packages	Substrate flatness Co-planarity of chip-to-package and package-to-board

* CTE—coefficient of thermal expansion

** UBM—under bump metallurgy

† EMI—electromagnetic interference

‡ EDA—electronic design automation

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Table 59a Assembly & Packaging Technology Requirements—Near Term**

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
<i>Cost (Cents/Pin) [A]</i>							
Low cost	0.40–0.90	0.38–0.86	0.36-0.81	0.34-0.77	0.33-0.73	0.31-0.70	0.29-0.66
Hand-held	0.50–1.30	0.48- 1.00	0.45- 0.95	0.43-0.90	0.41-0.86	0.39-0.82	0.37-0.78
Cost-performance	0.90–1.90	0.86- 1.40	0.81- 1.33	0.77-1.26	0.73-1.20	0.70-1.14	0.66-1.08
High-performance	3.10	2.95	2.80	2.66	2.52	2.40	2.28
Harsh	0.50–1.00	0.48–0.95	0.45–0.90	0.43-0.86	0.41-0.81	0.39-0.77	0.37-0.74
Memory	0.40–1.90	0.38–1.71	0.36–1.54	0.34–1.39	0.33–1.25	0.31–1.12	0.29–1.01
<i>Chip Size (mm²)</i>							
Low cost	53	55	57	59	61	63	65
Hand-held	53	55	57	59	61	63	65
Cost-performance	170	170	170	178	186	195	204
High-performance	310	310	310	325	340	356	372
Harsh	53	55	57	59	61	63	65
Memory	131	129	127	141	157	175	147
<i>Power: Single-Chip Package (Watts) [B]</i>							
Low cost	n/a	n/a	N/a	n/a	n/a	n/a	n/a
Hand-held	1.4	1.7	2.0	2.1	2.3	2.4	2.6
Cost-performance	48	54	61	75	81	88	96
High-performance	90	108	130	140	150	160	170
Harsh	14	14	14	14	14	14	14
Memory	0.8	1.0	1.2	1.4	1.6	1.8	2

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Table 59a Assembly & Packaging Technology Requirements—Near Term (continued)**

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
<i>Core Voltage (Volts)</i>							
Low cost	1.8	1.8	1.5	1.5	1.2	1.2	1.1
Hand-held	1.5	1.5	1.2	1.2	0.9	0.9	0.8
Cost-performance	1.8	1.8	1.5	1.5	1.2	1.2	1.1
High-performance	1.8	1.8	1.5	1.5	1.2	1.2	1.1
Harsh	5.0	3.3	3.3	3.3	2.5	1.8	1.8
Memory	1.8	1.8	1.5	1.5	1.2	1.2	1.1
<i>Package Pincount</i>							
Low cost	80–290	86–313	90–338	101–365	109–395	118–426	127–460
Hand-held	128–368	138–397	149–429	161–464	174–501	188–541	203–584
Cost-performance	370–740	400–821	432–912	466–1012	503–1123	544–1247	587–1384
High-performance [C]	1600	1792	2007	2248	2518	2820	3158
Harsh	40–240	40–259	40–280	40–302	40–327	40–353	40–381
Memory	44–128	44–128	44–128	44–144	44–144	48–160	48–160
<i>Overall Package Profile (mm)</i>							
Low cost	1.7	1.7	1.2	1.2	1.2	1.0	1.0
Hand-held	1.2	1.2	1.0	1.0	1.0	0.8	0.8
Cost-performance	1.2–1.7	1.2–1.7	1.0–1.2	1.0–1.2	1.0–1.2	0.8–1.0	0.8–1.0
High-performance	n/a	n/a	N/a	n/a	n/a	n/a	n/a
Harsh	1.4	1.4	1.0	1.0	1.0	1.0	1.0
Memory	1.2	1.2	1.0	1.0	1.0	0.8	0.8

Solutions Exist

Solutions Being Pursued

No Known Solutions

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Table 59a Assembly & Packaging Technology Requirements—Near Term (continued)**

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
<i>Performance: On-Chip (MHz)</i>							
Low cost	300	350	415	460	510	570	633
Hand-held	300	350	415	460	510	570	633
Cost-performance	600	693	800	890	989	1100	1225
High-performance	1200	1386	1600	1724	1857	2000	2155
Harsh	25	40	60	60	60	60	60
Memory (D/SRAM)	133/300	166/347	166/400	200/445	200/495	200/550	200/613
<i>Performance: Chip-to-Board for Peripheral Buses (MHz)</i>							
Low cost	75	75	100	100	100	100	100
Hand-held	75	75	100	100	100	100	100
Cost-performance [D]	133/300	166/347	166/400	200/445	200/495	200/550	200/613
High-performance [E]	480	693	800	862	929	1000	1078
Harsh	25	40	60	60	60	60	60
Memory (D/SRAM) [D]	133/300	166/347	166/400	200/445	200/495	200/550	200/613
<i>Junction Temperature Maximum (°C) [F]</i>							
Low cost	125	125	125	125	125	125	125
Hand-held	115	100	100	100	100	100	100
Cost-performance	100	95	90	85	85	85	85
High-performance	100	95	90	85	85	85	85
Harsh	155	155	155	155	155	155	175
Memory	100	100	100	100	100	100	100
<i>Operating Temperature Extreme: Ambient (°C) [F]</i>							
Low cost	55	55	55	55	55	55	55
Hand-held	55	55	55	55	55	55	55
Cost-performance	45	45	45	45	45	45	45
High-performance	45	45	45	45	45	45	45
Harsh	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 170
Memory	55	55	55	55	55	55	55

Solutions Exist Solutions Being Pursued No Known Solutions

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Table 59b Assembly & Packaging Technology Requirements—Long Term**

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
<i>Cost (Cents/Pin) [A]</i>			
Low cost	0.25–0.57	0.22–0.49	0.19–0.42
Hand-held	0.32–0.74	0.27–0.70	0.23–0.67
Cost-performance	0.57–1.03	0.49–0.98	0.42–0.93
High-performance	1.95	1.68	1.44
Harsh	0.32–0.63	0.27–0.54	0.23–0.46
Memory	0.25–0.74	0.22–0.54	0.19–0.39
<i>Chip Size (mm²)</i>			
Low cost	72	81	90
Hand-held	72	81	90
Cost-performance	234	268	307
High-performance	427	489	561
Harsh	72	81	90
Memory	205	191	250
<i>Power: Single-Chip Package (Watts) [B]</i>			
Low cost	N/a	n/a	n/a
Hand-held	2.1	2.3	2.5
Cost-performance	104	109	115
High-performance	171	177	186
Harsh	14	14	14
Memory	2.5	3.0	3.5
<i>Core Voltage (Volts)</i>			
Low cost	0.9	0.6	0.6
Hand-held	0.6	0.5	0.3
Cost-performance	0.9	0.6	0.6
High-performance	0.9	0.6	0.6
Harsh	1.8	1.8	1.8
Memory	0.9	0.6	0.6

Solutions Exist



Solutions Being Pursued



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Table 59b Assembly & Packaging Technology Requirements—Long Term (continued)**

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
<i>Package Pincount</i>			
Low cost	160–580	201–730	254–920
Hand-held	256–736	322–927	406–1167
Cost-performance	740–1893	932–2589	1174–3541
High-performance [C]	4437	6234	8758
Harsh	40–480	40–604	40–761
Memory	48–182	48–200	48–220
<i>Overall Package Profile (mm)</i>			
Low cost	1.0	1.0	1.0
Hand-held	0.65	0.65	0.5
Cost-performance	0.65–0.8	0.65–0.8	0.5–0.65
High-performance	N/a	n/a	n/a
Harsh	1.0	1.0	1.0
Memory	0.65	0.65	0.5

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Table 59b Assembly & Packaging Technology Requirements—Long Term (continued)

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
<i>Performance: On-Chip (MHz)</i>			
Low cost		840	1044
Hand-held		840	1044
Cost-performance		1522	1925
High-performance		2655	3190
Harsh		100	100
Memory (D/SRAM)		250/761	250/963
<i>Performance: Chip-to-Board for Peripheral Buses (MHz)</i>			
Low cost		125	125
Hand-held		125	125
Cost-performance [D]		250/761	250/963
High-performance [E]		1328	1595
Harsh		100	100
Memory (D/SRAM) [D]		250/761	250/963
<i>Junction Temperature Maximum (°C) [F]</i>			
Low cost		125	125
Hand-held		100	100
Cost-performance		85	85
High-performance		85	85
Harsh		185	185
Memory		100	100
<i>Operating Temperature Extreme: Ambient (°C) [F]</i>			
Low cost		55	55
Hand-held		55	55
Cost-performance		45	45
High-performance		45	45
Harsh		-40 to 180	-40 to 180
Memory		55	55

Solutions Exist



Solutions Being Pursued



No Known Solutions



Notes for Table 59 for Assembly and Packaging Requirements

[A] All costs do not include silicon, heat sinks, or test; substrate cost should not exceed 30–50% of total cost. Data shown are for 2 layer BGA vs. 4 layer BGA respectively. The requirement to remove Pb, Sb, and Br from packaging materials could increase costs 10-15% above present levels; there are currently no known solutions to meeting the cost challenges given this requirement for the Low Cost, Hand Held, Harsh, and Memory segments.

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- [B] Solutions are being pursued for cost-performance ≥ 75 W and for high-performance ≥ 130 W due to cost-driven thermal management issues. Cost-performance data is for desktop applications; notebook applications are limited to 14 W maximum in 1999. The memory power is for the SRAM chip.
- [C] The high-performance IC may be classified into two categories. The application-specific integrated circuit (ASIC) has a high number of signal I/O pins. The total number of voltage/ground pins is about one half of the number of signal I/O pins. The microprocessor has signal I/O pins much less than that of the ASIC; however, the power consumption of the microprocessor is much higher than that of the ASIC. Even with such a high number of voltage/ground pins, the effective overall inductance is still very high. On-chip de-coupling capacitance is needed. Ideally, one may want to place an on-chip de-coupling capacitance, $C(\text{de-coupling}) \approx 9 \text{ Power} / \{f(\text{on-chip}) \times [\text{Core Voltage}]^2\}$. Such consideration also applies to many of the high power cost-performance applications.
- [D] xx/yyy refers to system memory and peripheral bus speed (xx) and to processor cache memory data transfer (yyy) for high end of cost-performance category. Memory performance must match the requirements of processor buses and may require new architectures at the device or array level, such as reduced-width multiplexed buses that run at the on-chip frequency. **DDR and other high performance memory designs are not addressed and will be added in the 2001 update.**
- [E] > 1000 MHz reflects need for improved impedance control.
- [F] Uncertain materials solutions. Reflects package/substrate cost issues.

Table 60 Current Limits of 63Sn/37Pb Flip Chip Solder Bumps**

		Current Limits for 100,000 hour MTTF at Average Bump Temperatures of	
Bump Pitch	Passivation Opening	100°C	
250 μm	85 μm	150 mA	
200 μm	80 μm	130 mA	
150 μm	65 μm	90 mA	

Note: The electromigration limits for 63Sn/Pb solder is still being determined for junction temperatures in the range of 85 to 115°C. The data represented in Table 60 is a 2x improvement over the 1999 roadmap. A more complete update will be provided in the 2001 roadmap.

Table 61a Chip-to-Next Level Interconnect Potential Solutions—Near Term**

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Chip Interconnect Pitch (μm)							
Wire bond—ball	50	50	45	35	30	25	20
Wire bond—wedge	45	45	40	35	30	25	20
Flip Chip on Tape	50	50	40	40	40	40	30
Flip chip (area array) for cost-performance and high-performance	200	200	175	175	150	150	130
Flip chip for handheld, low cost, and harsh	180	165	150	130	120	110	100

Note: The Chip Interconnect Pitch for area array flip chip in cost-performance and high-performance market segments have been changed from those of ITRS 1999. The corresponding changes in Table 65 will be provided in the 2001 Roadmap.

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*Table 61b Chip-to-Next Level Interconnect Potential Solutions—Long Term***

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
<i>Chip Interconnect Pitch (μm)</i>			
Wire bond—ball		20	20
Wire bond— wedge		20	20
Flip Chip on Tape		30	30
Flip chip (area array) for cost- performance and high-performance		115	100
Flip chip for handheld, low cost, and harsh		70	40

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