ITRS/ORTC Table Update

Technology Node, DRAM Chip Size, and Logic Chip Size Update Proposal

ITRS 2000 Update

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ITRS Table Definitions/Guidelines

- Technology Requirements Perspective
  - Near-Term Years : First Yr. Ref.+6 yrs F'cast (ex. 1999 through 2005), annually
  - Long-Term Years : Following 9 years (ex.2008, 2011, and 2014), every 3 years
- Technology Node :
  - General indices of technology development.
  - Approximately 70 percent reduction of the preceding node.
  - Each step represents the creation of significant technology progress
  - DRAM half pitches of 180, 130, 100, 70, 50 and 35 nm

  *Year 2000 : Smallest 1/2 pitch among DRAM, ASIC, MPU, etc
- Year of Production Manufacturing :
  - The volume = *10K units (devices)/month. ASICs manufactured by same process technology are granted as same devices
  - Beginning of manufacturing by *a company and another company starts production within 3 months
- Technology Requirements Color :
  - Red : Good** potential solutions are NOT known
  - Yellow : Good** potential solutions are known, but it is not known which ones will be real solutions.
  - White : Good** potential solutions exist, and they are under optimization

  *Year 2000 : Red cannot exist in next 3 years (2000, 2001, 2002)***

  *Year 2000 : Yellow cannot exist in next 1 year (2000)

** "Good" = "Ready for Production manufacturing"

*** Exception: "Does not prevent Production(DRAM), Ramp(MPU) manufacturing."

Summary of Key Assumption Proposed Changes WAS(1999 ITRS) vs. IS(Proposal) (Technology Node):

Technology Node Assumptions:

a) DRAM Half-Pitch

WAS: 1999/180 , 2000/165, 2001/150, 2002/130, 2003/120, 2004/110, 2005/100,2008/70, 2011/50, 2014/35

IS [1] with 130nm pull-in and interpolation to 2005/100nm:

1999/180, 2000/165, 2001/130, 2002/120, 2003/115, 2004/105, 2005/100,2008/70, 2011/50, 2014/35

IS [2] with 130nm pull-in and 70% reduction:

1999/180, 2000/165, 2001/130, 2002/115, 2003/105, 2004/90, 2005/80,2008/60, 2011/40, 2014/30

b) ASIC/MPU Half-Pitch:

WAS: MPU/ASIC Half Pitch Same, lagged typically 2 years behind DRAM

IS: **MPU/ASIC line item tracking,** 1999-2005 same as 1999 ITRS, **MPU/ASIC accelerates to DRAM level after 2005**

Summary of Key Assumption Proposed Changes WAS(1999 ITRS) vs. IS(Proposal) (Technology Node):

Technology Node Assumptions:

c) MPU Gate Length:

WAS: MPU Gate Length (Printed in Photoresist and Etched in Polysilicon) Same as 1999 ITRS except:

IS: 1. MPU Variable ranges in 2002, 2011, 2014 replaced by single targets; 2. NEW: MPU/ASIC Bottom Gate Length (Final Physical Post-Etch) line item targets added which are pulled-in 1 year from Lithography "In Resist" targets. FEP, PIDs, Design TWGs to add to their tables.

d) ASIC Gate Length:

WAS: ASIC Gate Length (Printed in Photoresist and Etched in Polysilicon) typically lagged 1 node behind MPU.

IS: MPU/ASIC matches MPU Gate Lengths (Both Printed Gate Length and new Post-Etch Bottom Gate Length) starting 1999.

Summary of Key Assumption Proposed Changes WAS(1999 ITRS) vs. IS(Proposal) (cont.- DRAM):

DRAM Assumptions:

a) Cell Area Factor Limits (from FEP TWG):

WAS: 8x/1999 -> 6x/2002 -> 4.4x/2005 -> 3.0x/2011 -> 2.5x/2014

IS: 8x/1999-2004, 6x/2005-2010, 4x/2011-16

b) Cell Array Efficiency Limit Trends (from FEP, Nikkei Microdevices):

WAS:	Intro:	1999/70%	--> 2016/75%
IS:	**Intro:**	**1999/70%**	**--> 2016/75%**
WAS:	Production	1999/53%	--> 2016/57%
IS:	**Production**	**1999/53%**	**--> 2016/58%**

c) Litho Field Size Maximum Limit (from Litho TWG):

WAS: 4x Magnification, 6-inch Reticle

Intro	**1999-2016**	**25x32 = 800mm2**
Production	**1999-2016**	**12.5x32 = 400mm (2 chips/field)**

IS: 5x Magnification, 6-inch Reticle

Intro	**1999-2016**	**22x26 = 572mm2**
Production	**1999-2016**	**11x26 = 286mm2 (2 chips/field)**

d) Bits/Chip Product Generation Growth Rate:

WAS:	1999-2014:	2x bits/chip every 2 years
IS:	**Through 2Gbit:**	**2x bits/chip every 2 years;**
	After 2Gbit:	**2x bits/chip every 2-3 years (4x/5years)**

Summary of Key Assumption Proposed Changes WAS(1999 ITRS) vs. IS(Proposal) (cont.- Logic):

MPU Assumptions:

a) High Performance (HP) MPU @Ramp Starting Chip Size:

WAS: 2Mbyte on-chip (6t) SRAM in 1999
(170mm2 Core plus 280mm2 SRAM = 450mm2/1999)

IS: 1Mbyte on-chip (6t) SRAM in 1999
(170mm2 Core plus 140mm2 SRAM = 310mm2/1999)

b) Cost Performance (CP) Starting Chip Size (SAME as 1999 ITRS):

MPU @Introduction/340mm2

MPU @Ramp/170mm2

c) SRAM and Logic Transistors/chip Trend (SAME as ITRS) = 2x/2yrs

d) Chip Size Growth Rate Trend

WAS: Flat chip sizes through 2001, then 1.2x/4rs

IS: Both HP and CP MPU grow at 1.2x/4yrs starting 1999

DRAM Chip Size Proposal("IS") vs. 1999 ITRS("WAS")

			4x/4yr (2G generation) 4x/5yr (after)							
	Cell Factor		Proposal		ITRS '99					ITRS '99
Year	IS	WAS	Intro	Size	WAS	WAS		Prod	Size	WAS	WAS
1999	8.0	8.0	1G	400	1G	400		256M	131	256M	132
2000	8.0	7.3									
2001	8.0	6.6	2G	548	2G	438		512M	179	512M	145
2002	8.0	6.0									
2003	8.0	5.4	4G	691	4G	480		1G	225	1G	159
2004	8.0	4.9	4G	578							
2005	6.0	4.4			8G	526		2G	231	2G	174
2006	6.0	4.1	8G	575							
2007	6.0	3.8			[16G]			4G	293	[4G]	
2008	6.0	3.5	16G	689	[22.6G]	603		4G	222	[5.7G]	199
2009	6.0	3.3	16G	504	[32G]					[8G]	
2010	6.0	3.2						8G	272		
2011	4.0	3.0	32G	464	64G	691				16G	229
2012	4.0	2.8						16G	236		
2013	4.0	2.7	64G	582	[128G]					[32G]	
2014	4.0	2.5			[181G]	792				[45.2G]	262
2015	4.0	2.5						32G	235		
2016	4.0	2.5	128G	579							

Table 1a Product Generations and Chip Size Model—Near Term Years

YEAR OF PRODUCTION TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Lithography-Based Characteristics								
DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch (nm) IS [1] with 130nm pull-in and interpolation to 2005/100nm:	180	165	130	120	115	105	100	D ½
DRAM ½ Pitch (nm) IS [2] with pull-in and 70% reduction	180	165	130	115	105	90	80	D ½
MPU/ASIC ½ Pitch (nm) WAS	230	210	180	160	145	130	115	M AND A ½
MPU/ASIC ½ Pitch (nm)) IS [1] SAME AS DRAM [1] AFTER 2005	230	210	180	160	145	130	115	M AND A ½
MPU/ASIC ½ Pitch (nm)) IS [2] SAME AS DRAM [2] AFTER 2005	230	210	180	160	145	130	115	M AND A ½
MPU Gate Length (nm) †† WAS	140	120	100	85-90	80	70	65	M GATE
ASIC Gate Length (nm) WAS	180	165	150	130	120	110	100	A GATE
MPU/ASIC Gate Length (In Resist) (nm) †† IS	140	120	100	90	80	70	65	M AND A GATE
Physical Bottom Gate-Length								
MPU/ASIC Gate Length (nm) †† NEW	120	100	90	80	70	65	60	COST/PERFORMANCE

⋯⋯ => Roadmap portion still under discussion

ITRS 2000 Update Work In Progress - Do Not Publish!

Table 1b Product Generations and Chip Size Model—Long Term Years

YEAR OF PRODUCTION TECHNOLOGY NODE	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Lithography-Based Characteristics			
DRAM ½ Pitch (nm)	70	50	35
DRAM ½ Pitch (nm) IS **[1]** **with 130nm pull-in and interpolation to 2005/100nm:**	70	50	35
DRAM ½ Pitch (nm) IS **[2]** **with pull-in and 70% reduction**	60	40	30
MPU/ASIC ½ Pitch (nm) **WAS**	80	55	40
MPU/ASIC ½ Pitch (nm)) IS **[1] SAME AS DRAM [1]** **AFTER 2005**	**70**	**50**	**35**
MPU/ASIC ½ Pitch (nm)) IS **[2] SAME AS DRAM [2]** **AFTER 2005**	**60**	**40**	**30**
MPU Gate Length (nm) †† **WAS**	45	30-32	20-22
ASIC Gate Length (nm) **WAS**	70	50	35
MPU/ASIC Gate Length **(In Resist)** *(nm)* †† **IS**	**45**	**33**	**22**

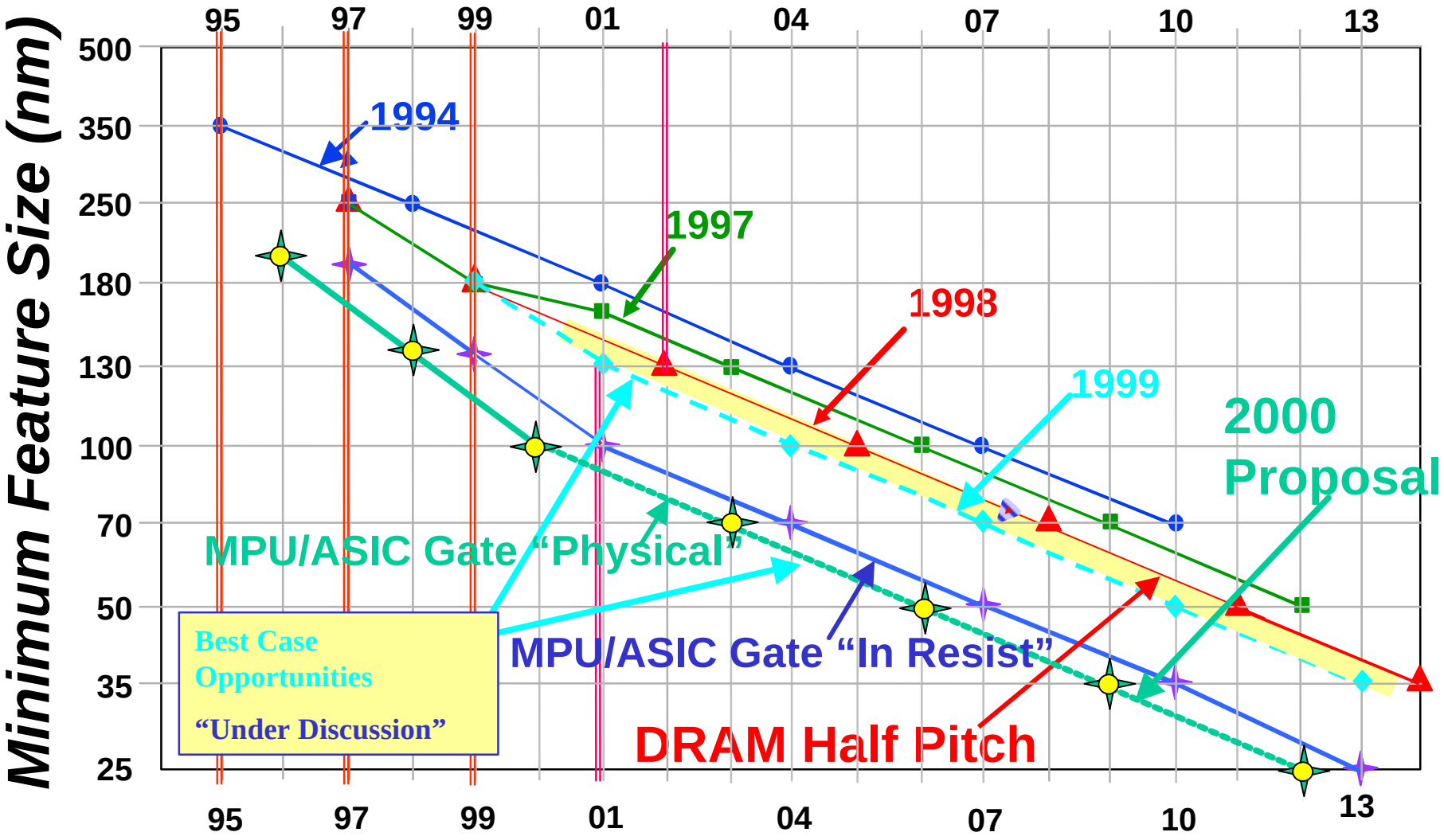
Physical Bottom Gate-Length			
MPU/ASIC *Gate Length (nm)* †† **NEW**	**40**	**30**	**20**

=> Roadmap portion still under discussion

ITRS 2000 Update Work In Progress - Do Not Publish!

ITRS Roadmap Acceleration Continues

(Including MPU/ASIC "Physical Gate Length" Proposal)



Chip Size - Model Assumptions, Notes, Tables

Table 1a Product Generations and Chip Size Model—[Assumptions, Notes]

†† **WAS:** *Range of [MPU Gate-Length] node targets indicates the acknowledgment of the difficulty of projecting the impact of the return to the 3-year technology node cycle starting in 2001 and the uncertainty of the long term years of the Roadmap timeframe.*

†† **IS: [No Ranges in cells]. MPU and ASIC Gate-length (In Resist) node targets refer to most aggressive requirements, as printed in photoresist** *(which was by definition also "as etched in polysilicon", in the 1999 ITRS).* **Trends have been identified, in which the "Final Physical" MPU and ASIC bottom gate lengths (Post-Etch) may be reduced from the as-printed dimension through linewidth-control etching. These etch-controlled "final physical" bottom gate-length targets are also included in the FEP, PIDs, and Design TWG Tables as Device and Etch technology requirements.**

§ **WAS:** *DRAM Model—Generations 4´ bits/chip every four years with interim 2´ bits/chip generations; InTER-generation chip size growth rate model is 1.2´ every four years; InTRA-generation chip size shrink model is 0.5´ every three years beginning 1999.*

§ **IS:** *DRAM Model—***Cell Factor (design/process improvement) targets are: 1999-2004/8x; 2005-2010/6x; 2011-2016/4x.** *Generations 4´ bits/chip every four years with interim 2´ bits/chip generations* **through 2G generation, then 4x/5years (2x/2-3yrs).** *InTER-generation chip size growth rate* **varies to maintain 1 die per 572mm2 field at Introduction and 2 die per 572mm2 field at Production.** *InTRA-generation chip size shrink model is 0.5´* **every technology node between cell factor shrinks.**

Chip Size - Model Assumptions, Notes, Tables (cont. - MPU)

Table 1a Product Generations and Chip Size Model— [Assumptions, Notes]

† **WAS/IS:** p is processor, numerals reflect year of introduction, c is cost-performance product.

‡ **WAS/IS:** p is processor, numerals reflect year at ramp, h is high-performance product.

* **WAS/IS:** MPU Cost-performance Model— Cost-performance MPU includes small level 1 (L1) on-chip SRAM (32Kbyte/1999), but consists primarily of logic transistor functionality; both SRAM and Logic functionality doubles every two years.

** **WAS:** MPU High-performance Model— High-performance MPU includes large level 2 (L2) on-chip SRAM (2MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + 98M transistors (2048 bytes ´ 8 bits/byte ´ 6 transistors/bit) L2 SRAM = 110M transistors/1999); both SRAM and Logic functionality doubles every two years.

** **IS:** MPU High-performance Model— High-performance MPU includes large level 2 (L2) on-chip SRAM (**1**MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + **49**Mtransistors (1024 bytes ´ 8 bits/byte ´ 6 transistors/bit) L2 SRAM = **61**Mtransistors/1999); both SRAM and Logic functionality doubles every two years.

*** **WAS:** MPU Chip Size Model— Both the cost-performance and high-performance MPUs target for InTER-generation chip size growth rate model is flat through 2001, then 1.2´ growth every four years after 2001; InTRA-generation chip size shrink model is 0.5´ every two years through 2001, then 0.5´ every three years after 2001.

*** **IS:** MPU Chip Size Model— Both the cost-performance and high-performance MPUs **use an** InTER-generation chip size growth rate model **which is** 1.2´ growth every four years **beginning 1999**; InTRA-generation chip size shrink model is 0.5´ every **technology node eginning 1999**.

Table 1a Product Generations and Chip Size Model—Near Term Years

YEAR OF PRODUCTION / *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*DRIVER*
DRAM ½ Pitch **[f]** *(nm)*	180	165	150	130	120	110	100	*D ½*
Memory (cont.)								
Cell area factor **[A]** **WAS**	8.0	7.3	6.6	6.0	5.4	4.9	4.4	*Market — Cost/Timing*
Cell area factor **[A]** **IS**	8.0	**8.0**	**8.0**	**8.0**	**8.0**	**8.0**	**6.0**	*Market — Cost/Timing*
Cell area **[Ca = Af²]** *(mm^2)* **WAS**	0.26	0.20	0.15	0.10	0.08	0.059	0.044	*Market — Cost/Timing*
Cell area **[Ca = Af²]** *(mm^2)* **IS**	**0.259**	**0.218**	**0.180**	**0.135**	**0.115**	**0.097**	**0.060**	*Market — Cost/Timing*
Generation at production § **WAS/IS**	256M	—	512**M**	—	1G	—	2G	*Market — Cost/Timing*
Functions per chip (Gbits) **NEW**	**0.268**	**0.380**	**0.537**	**0.759**	**1.07**	**1.52**	**2.15**	*Market —* **Cost/Timing**
Chip size at production (mm^2) § **WAS**	132	—	145	—	159	—	174	*Market — Cost/Timing*
Chip size at production (mm^2) § **IS**	**131**	**154**	**179**	**188**	**225**	**265**	**231**	*Market — Cost/Timing*
Cell array area at production (% of chip size) § **WAS**	53%	—	55%	—	53%	—	54%	*Market — Cost/Timing*
Cell array area at production (% of chip size) § **IS**	**53.0%**	**53.5%**	**54.1%**	**54.7%**	**55.1%**	**55.4%**	**55.8%**	*Market — Cost/Timing*
Gbits/cm^2 at production § **WAS**	0.20	—	0.37	—	0.68	—	1.23	*Market — Cost/Timing*
Gbits/cm^2 at production § **IS**	**0.20**	**0.25**	**0.30**	**0.40**	**0.48**	**0.57**	**0.93**	*Market — Cost/Timing*

Table 1b Product Generations and Chip Size Model—Long Term Years

YEAR OF PRODUCTION / *TECHNOLOGY NODE*		*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
DRAM ½ Pitch **[f]** *(nm)*		70	50	35
Memory				
Cell area factor **[A]**	**WAS**	3.5	3.0	2.5
Cell area factor **[A]**	**IS**	**6.0**	**4.0**	**4.0**
Cell area **[Ca = Af²]** *(mm²)*	**WAS**	0.017	0.008	0.003
Cell area **[Ca = Af²]** *(mm²)*	**IS**	**0.0294**	**0.0100**	**0.0050**
Generation at production §	**WAS**	[5.7]	16G	[45.2G]
Generation at production §	**IS**	**4G**	**10.6G**	**24.2G**
Functions per chip (Gbits)	**NEW**	**4.3**	**11.3**	**26.0**
Chip size at production (mm²) §	**WAS**	199	229	262
Chip size at production (mm²) §	**IS**	**222**	**197**	**225**
Cell array area at production (% of chip size) §	**WAS**	52%	56%	57%
Cell array area at production (% of chip size) §	**IS**	**56.8%**	**57.5%**	**58.0%**
Gbits/cm² at production §	**WAS**	3.05	7.51	18.5
Gbits/cm² at production §	**IS**	**1.93**	**5.75**	**11.6**

Table 1a Product Generations and Chip Size Model—Near Term Years

YEAR OF PRODUCTION TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM ½ Pitch (nm) [f]	180	165	150	130	120	110	100	D ½
Memory								
Cell area factor [A] WAS	8.0	7.3	6.6	6.0	5.4	4.9	4.4	Market — Cost/Timing
Cell area factor [A] IS	8.0	8.0	8.0	8.0	8.0	8.0	6.0	Market — Cost/Timing
Cell area [Ca = Af²] (mm^2) WAS	0.26	0.20	0.15	0.10	0.08	0.059	0.044	Market — Cost/Timing
Cell area [Ca = Af²] (mm^2) IS	0.259	0.218	0.180	0.135	0.115	0.097	0.060	Market — Cost/Timing
Generation at introduction § WAS	1G	—	2G	—	4G	—	8G	—
Generation at introduction § IS	1G	—	2G	—	—	4G	—	—
Functions per chip (Gbits) WAS	1.07	—	2.15	—	4.29	—	8.59	Market — Moore's Law
Functions per chip (Gbits) IS	1.07	—	2.15	—	—	4.29	—	Market — Cost/Timing
Chip size at introduction (mm^2) § WAS	400	—	438	—	480	—	526	Market — Cost/Timing
Chip size at introduction (mm^2) § IS	400	—	548	—	—	578	—	Market — Cost/Timing
Cell array area at introduction (% of chip size) § WAS	70%	—	72%	—	70%	—	72%	Market — Cost/Timing
Cell array area at introduction (% of chip size) § IS	69.5%	70.0%	70.6%	71.2%	71.6%	71.9%	72.3%	Market — Cost/Timing
Gbits/cm^2 at introduction § WAS	0.27	—	0.49	—	0.89	—	1.63	Market — Cost/Timing
Gbits/cm^2 at introduction § IS	0.27	—	0.39	—	—	0.74	—	Market — Cost/Timing

Table 1b Product Generations and Chip Size Model—Long Term Years

YEAR OF PRODUCTION / *TECHNOLOGY NODE*		*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
DRAM ½ Pitch (nm) **[f]**		70	50	35
Memory				
Cell area factor **[A]**	**WAS**	3.5	3.0	2.5
Cell area factor **[A]**	**IS**	**6.0**	**4.0**	**4.0**
Cell area **[Ca = Af²]** *(mm^2)*	**WAS**	0.017	0.008	0.003
Cell area **[Ca = Af²]** *(mm^2)*	**IS**	**0.0294**	**0.0100**	**0.0050**
Generation at introduction §	**WAS**	[22.6G]	64G	[181G]
Generation at introduction §	**IS**	**[13.9G]**	**32G**	**[73.5G]**
Functions per chip (Gbits)	**WAS**	24.3	68.7	194
Functions per chip (Gbits)	**IS**	**15.0**	**34.4**	**78.9**
Chip size at introduction (mm^2) §	**WAS**	603	691	792
Chip size at introduction (mm^2) §	**IS**	**600**	**464**	**530**
Cell array area at introduction (% of chip size) §	**WAS**	69%	75%	75%
Cell array area at introduction (% of chip size) §	**IS**	**73.3%**	**74.0%**	**74.5%**
Gbits/cm^2 at introduction §	**WAS**	4.03	9.94	24.5
Gbits/cm^2 at introduction §	**IS**	**2.49**	**7.40**	**14.9**

Table 1a Product Generations and Chip Size Model— Near Term Years

YEAR OF PRODUCTION TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Logic (High-volume Microprocessor) Cost-performance *								
Process/design annual improvement factor ++	0.90	0.90	0.90	0.91	0.92	0.93	0.93	Market — Cost/Timing
IS	**0.90**	**0.93**	**0.93**	**0.93**	**0.93**	**0.93**	**0.93**	
Transistor density SRAM at introduction (M transistors/cm ^{2})	35	50	70	95	128	173	234	Market — Cost/Timing
IS	**35**	**47**	**64**	**87**	**117**	**158**	**213**	
Transistor density logic at introduction (M transistors/cm ^{2})	6.6	9.4	13	18	24	33	44	Market — Cost/Timing
IS	**6.6**	**9.0**	**12.1**	**16.4**	**22.1**	**29.9**	**40.4**	
Generation at introduction †	p99c	—	p01c	—	p03c	—	p05c	—
Functions per chip (million transistors [M transistors])	23.8	—	47.6	—	95.2	—	190	Market — Moore's Law
Chip size at introduction (mm ^{2}) ***	340	—	340	—	372	—	408	Market — Cost/Timing
IS	**340**	**356**	**372**	**390**	**408**	**427**	**447**	
Cost performance MPU (M transistors/cm ^{2} at introduction) (including on-chip SRAM) ***	7	—	14	—	26	—	47	M Gate and M and A ½
IS	**7.0**	**9.5**	**12.8**	**17.3**	**23.3**	**31.5**	**42.6**	
Generation at production †	p97c	—	p99c	—	p01c	—	P03c	—
Chip size at production (mm ^{2}) ***	170	—	170	—	214	—	235	Market — Cost/Timing
IS	**170**	**178**	**186**	**195**	**204**	**214**	**223**	
Cost performance MPU (M transistors/cm ^{2} at production, including on-chip SRAM) ***	7	—	14	—	22	—	41	M Gate and M and A ½
IS	**7.0**	**9.5**	**12.8**	**17.3**	**23.3**	**31.5**	**42.6**	

++ The MPU Process/design improvement factor is an estimate of the additional annual functional area reduction required beyond the area reduction contributed by the MPU metal half-pitch reduction. Note that this additional area reduction for transistor density plays a role generally analogous to the "cell area factor" for DRAMs. It has been achieved historically through a combination of many factors, for example: use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout.

Table 1b Product Generations and Chip Size Model—Long Term Years

YEAR OF PRODUCTION TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
*Logic (High-volume Microprocessor) Cost-performance **			
Process/design improvement factor	0.93	0.93	0.93
IS	**0.93**	**0.93**	**0.93**
Transistor density SRAM at introduction (Mtransistors/cm^2)	577	1,423	3,510
IS	**526**	**1,299**	**3,204**
Transistor density logic at introduction (Mtransistors/cm^2)	109	269	664
IS	**100**	**245**	**606**
Generation at introduction †	—	p11c	—
Functions per chip (million transistors (Mtransistors))	539	1,523	4,308
*Chip size at introduction (mm^2) ****	468	536	615
IS	**512**	**588**	**674**
*Cost-performance MPU Mtransistors/cm^2 at introduction (including on-chip SRAM) ****	115	284	701
IS	**105**	**259**	**640**
Generation at production †	—	p09c	—
*Chip size at production (mm^2) ****	269	308	354
IS	**256**	**294**	**337**
*Cost performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ****	100	247	609
IS	**105**	**259**	**640**

Table 1a Product Generations and Chip Size Model—Near Term Years (continued)

YEAR OF PRODUCTION TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Logic (Low-volume Microprocessor) High-performance **								
Generation at production ‡	p99h	—	p01h	—	p03h	—	p05h	—
Functions per chip (million transistors)	110	—	220	—	441	—	882	*Market — Moore's Law*
IS	**61**	**86**	**122**	**172**	**244**	**345**	**488**	
Chip size at production (mm^2) ***	450	—	450	—	567	—	622	*Market — Cost/Timing*
IS	**310**	**325**	**340**	**356**	**372**	**390**	**408**	
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ***	24	—	49	—	78	—	142	*M Gate and M and A ½*
IS	**20**	**27**	**36**	**49**	**66**	**89**	**120**	
ASIC								
ASIC usable Mtransistors/cm^2 (auto layout)	20	28	40	54	73	99	133	*M Gate and M and A ½*
IS	**20**	**27**	**36**	**49**	**66**	**89**	**120**	
ASIC max chip size at production (mm^2) (maximum lithographic field size)	800	800	800	800	800	800	800	*Lithographic Field Size*
IS	800	800	800	800	800	800	**572**	
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	160	224	320	432	584	800	1064	*Market — Performance/ Timing*
IS	160	**216**	**288**	**392**	**528**	**712**	**686**	

Table 1b Product Generations and Chip Size Model—Long Term Years (continued)

YEAR OF PRODUCTION TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Logic (Low-volume Microprocessor) High-performance **			
Generation at production ‡	—	p11h	—
Functions per chip (million transistors)	2,494	7,053	19,949
IS	**1,381**	**3,907**	**11,052**
Chip size at production (mm^2) ***	713	817	937
IS	**467**	**536**	**614**
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ***	350	863	2,130
IS	**296**	**729**	**1,798**
ASIC			
ASIC usable Mtransistors/cm^2 (auto layout)	328	811	2,000
IS	**296**	**729**	**1,798**
ASIC maximum chip size at production (mm^2) (maximum lithographic field size) **WAS**	800	800	800
IS	**572**	**572**	**572**
ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	2,624	6,488	16,000
IS	**1693**	**4170**	**10285**

Since only the 2011 odd-year product generation data column is available in the Long Term table format, interpolated numbers were calculated and included in the 2008 and 2014 node columns. The extended market-need-based product trends for the product generation two-year-cycle years (1999, 2001, 2003, 2005, 2007, 2009, 2011, 2013) are forecast to follow patterns established in Near Term Table 1a.