

ITWG Meeting, 4/11/00: Leuven, Belgium

PIDS TWG Report Out

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PIDS Internal Meeting Summary

- **2000 ITRS Table 28, 29, and 30 updates**
 - **Mainly minor updates, correction**
- **Key issues for 2001**
 - **Logic and memory**
 - Review ASIC gate length
 - Dynamic, circuit implications of gate leakage on logic
 - Review gate sheet resistance with Design
 - Review Vdd, Tox
 - Review low power spec's, perhaps add cellular
 - DRAM cell size, Tox dependent on IRC chip size, chip storage area decisions
 - **Analog**
 - General review to understand process/integration issues
 - **Reliability**
 - Review possible burn-in requirements and SOC requirements
- **Novel devices table: what to do with it?**

PIDS Cross-TWG Meetings

- **Strong interest in novel device impact**
- **General: cross-TWG issues important**
- **Design**
 - **2001: Static power dissipation is important unresolved issue: impacts systems, devices, and gate stack module**
 - **2001: Strong interaction on circuit and system issues needed**
- **Modeling & simulation**
 - **2001: gate stack and SOC modeling important**
- **FEP**
 - **Strong joint efforts needed and planned**
 - Flash
 - Expanded logic low power requirements
 - FERAM
- **Interconnect**
 - **Minor adjustment of shortwire pitch**
 - **Important joint issues with high K coupling, bypass, and other cap's**