

Technology Node Timing

- Lithography ITWG has not reached consensus on accelerating timing. Need clarification of:
 - Definition of node
 - Quantity of chips made/month... 10K, 50K?
 - Month in year... Jan, July, Dec?
 - How many chip makers?
 - Leading edge or average?
 - No “yellow”?
 - Clear statement of what progress has been made to turn “red” to “yellow”
 - Examination/assessment of when “red” will turn to “yellow” i.e. to pull 100nm node into 2004, will gate CDC be $\leq 6\text{nm}$?
 - Need to relook at MPU, ASIC half-pitch (and other requirements) versus DRAM. Maybe they should be accelerated.
- Targeting consensus before July ITWG meeting

Key Concerns for 2000 ITRS Update

6) New Devices (non-CMOS)

- Understand impact on lithography
- Start with single table in 2000 and expand definition in 2001
 - Need clearer input/requirement from IRC, other ITWGs
 - Check for cross-ITWG meeting on April 11, 2000.

Scanner Reduction Rate (SSR)

- ITWG recommends following issues be addressed at May 8th SSR Workshop organized by ISMT:
 - 1) What is the timing? node, year, wavelength?
 - 2) Comprehensive cost analysis
 - impact of throughput reduction
 - impact on mask industry, what real benefit do they get
 - does it help accelerate the roadmap?
 - 3) Complications of 4X, 5X/6X on leading edge mask making?
 - 4) Do all scanner suppliers have to agree? What if they don't?
 - 5) Impact on NGL? Must they follow? Especially EPL?

Action Items - Lithography ITWG Meeting

April 10, 2000

- 1) Send your membership list to other ITWGs - all
- 2) Ask IRC definition of the node/timing - J. Canning
- 3) Review SoC definition on page 23 and see how it applies to requirements (litho) on page 147 - All
- 4) Check with IRC that page 23 is still current - J. Canning
- 5) Ask IRC to give us an update of the ISMT GEF Workshop (and other related activities) now or at July meeting - J. Canning
- 6) Each ITWG to review Gil Shelden's mask/MEF proposal due in May, and feedback/comment to Gil by June 21st - All
- 7) Put mask/MEF on agenda for July Litho ITWG meeting to finalize/ratify proposal - J. Canning

System-on-Chip (SoC) Definition

- In Japan today, SoC is high performance logic so requirements should be tighter than ASIC.

Examples are DTV, games in “Playstation” (in general for most companies)

- In Taiwan emphasis is to define embedded DRAM with logic, i.e. need leading edge lithography for E-DRAM.

It is lower cost than MPU.

- Review SoC definition on page 23 and see how it applies to requirements (litho) on page 147 - AR for all.
- Check with IRC that page 23 is still current - J. Canning

Mask (MEF) and Defects

- Clarify table double entry
 - is it 248 PSM/193 BIN
 - 193 PSM/157 BIN, etc.?
- CD Uniformity for contacts
 - is it for BIN or half-tone (PCM)?
 - MEF factor actually increases faster than requirements table shows
(H. Levinson questionnaire can give input on above)
- Each ITWG to review - Gil Shelden's proposal due in May, and feedback/comments to Gil by June 21 - AR for all
- Put on agenda for July meeting to finalize/ratify proposal - AR for J. Canning