

# ITRS Meeting April 10-11, 2000

- FEP ITWG Participants
  - W. Class (US, Eaton Corp.)
  - L. Larson (US, Int. SEMATECH)
  - M. Alessandri (Europe, ST Microelectronics)
  - S. Kawamura (Japan, Fujitsu)
  - H. Tsai (Taiwan, Winbond)
  - H. Kang (Korea, Samsung)

# FEP Concerns/Actions by Year

- Y2000
  - DRAM Chipsize Resolution
    - Extra implications from die size implications vs 2 chips/Field exposure
    - Affects: Stack Capacitor Roadmap, Trench Capacitor Roadmap, Defect Roadmap
  - MPU Chipsize
    - Affects: Defect Requirements Roadmaps
  - General Node Changes
    - If there is a change - all of our tables change
  - Improve Content/Quality of the links
  - Not ready to comment to End-of-Roadmap Devices

# FEP Concerns/Actions by Year

- Y2001
  - High Priority Devices
    - 1) Flash EEPROM - - FEP/PIDS team defined - M.Alessandri(FEP)&S. Deleonibus(PIDS)
    - 2) Extended Logic MOSFET +embedded DRAM - - PIDS response promised - Kawamura-san(FEP)& (TBD) PIDS
    - 3) FeRAM - - PIDS response promised - Kawamura-san(FEP)& (TBD) PIDS
  - Unit Processes / Materials
    - Yield Model, Validation & Defect Forecasting
      - **FEP/DR Preliminary team leaders identified - Huff (FEP), Chris Long(DR)**
      - **Preliminary Meeting Scheduled ~ May 2000**
    - **PMD**
      - **FEP/Interconnect Team TBD - W.Class, Bob Geffin assignment**
    - **HiK Coupling Capacitor**
      - **FEP advises Interconnect as per materials choices for possible solutions**

# Agreement of FEP Groups from Japan and Korea to address DRAM sizing

- Message to the IRC:
- Japan and Korea FEP will optimize DRAM Sizing forecast for “a”, chip size, and density within the next 4 weeks
  - **DRAM 1/2 Pitch** Scales as per current ITRS
  - **Cell factor** “a” today = 8, Theoretical “a”=4 - - Achievement of “a”=4 set to 2011 [quantized by factors of 2 with 4”very difficult”]
  - We will allow **chip size** to grow <1.2X every 2 years
    - Chip size 132mm<sup>2</sup>@ production ramp (256MBit) is reasonable
  - Will allow **DRAM density** to grow <2X every 2 years
  - **Cell Area Efficiency** remains as per the present roadmap

# FEP/Interconnect/Litho /Metrology X-cut

- **FEP Topics** with Interconnect
  - PMD Module (FEP will cover - IC asks - does this mean planarization also - Yes ??)
  - HighK Coupling Capacitor - FEP will do [for other applications we provide assistance where needed- plus any other integrated HiK needs]
- **Metrology Topics:**
  - New Devices - FEP/Litho - notes that layers serve different functions - changes metrology needs
  - Trench sidewall slope/depth -
  - Dopant Conc. Gradient, Spatial Resolution
- **FEP Topics** with Litho
  - The DRAM “a” factor and approach- some resolution expected this afternoon

# FEP/PIDS X-cut

- **FEP Device Priorities**
  - 1-Flash memory, 2-Expanded Logic, 3-FeRAM
- PIDS owns electrical requirements - FEP owns unit processes and their requirements
- **Flash**
  - set up FEP/PIDS X-cut team to generate proposed requirements
- **Expanded Logic -**
  - proposes setting up 3 logic areas High Performance, Low Operation Power, Low Standby Power, + embedded DRAM
  - Discussion - electrical requirements are too stringent - design should carry some of this
  - PIDS will consider how to address this as their approach to the topic is different- Will get back to us

# FEP/Defect Reduction X-cut

- FEP requested meeting as Starting Materials and Surface Preparation are concerned about the validity of the defect yield model - over-aggressive???
- DRTWG and/or SEMATECH could do a rough survey as per “delta” - or kill factor - and active area ratio - validation in the form of a survey -
  - modeling is not a problem, it’s the assumptions
  - wafer suppliers need to be included in the team
- Will try to assemble a team to approach this. - Team: David/ Darron/? - perhaps Howard can get participants from the Starting Materials team to participate - Hold a meeting later to kick this off. - Chris Long agreed to be the initial point of contact for the meeting/group

# Modeling & Simulation / FEP X-cut meeting

- Modeling Request - Should we be allocating resources into Hi-K modeling ??
  - Yes - Referenced SEMATECH & NCSU & IMEC for guidance