Interconnect Working Group

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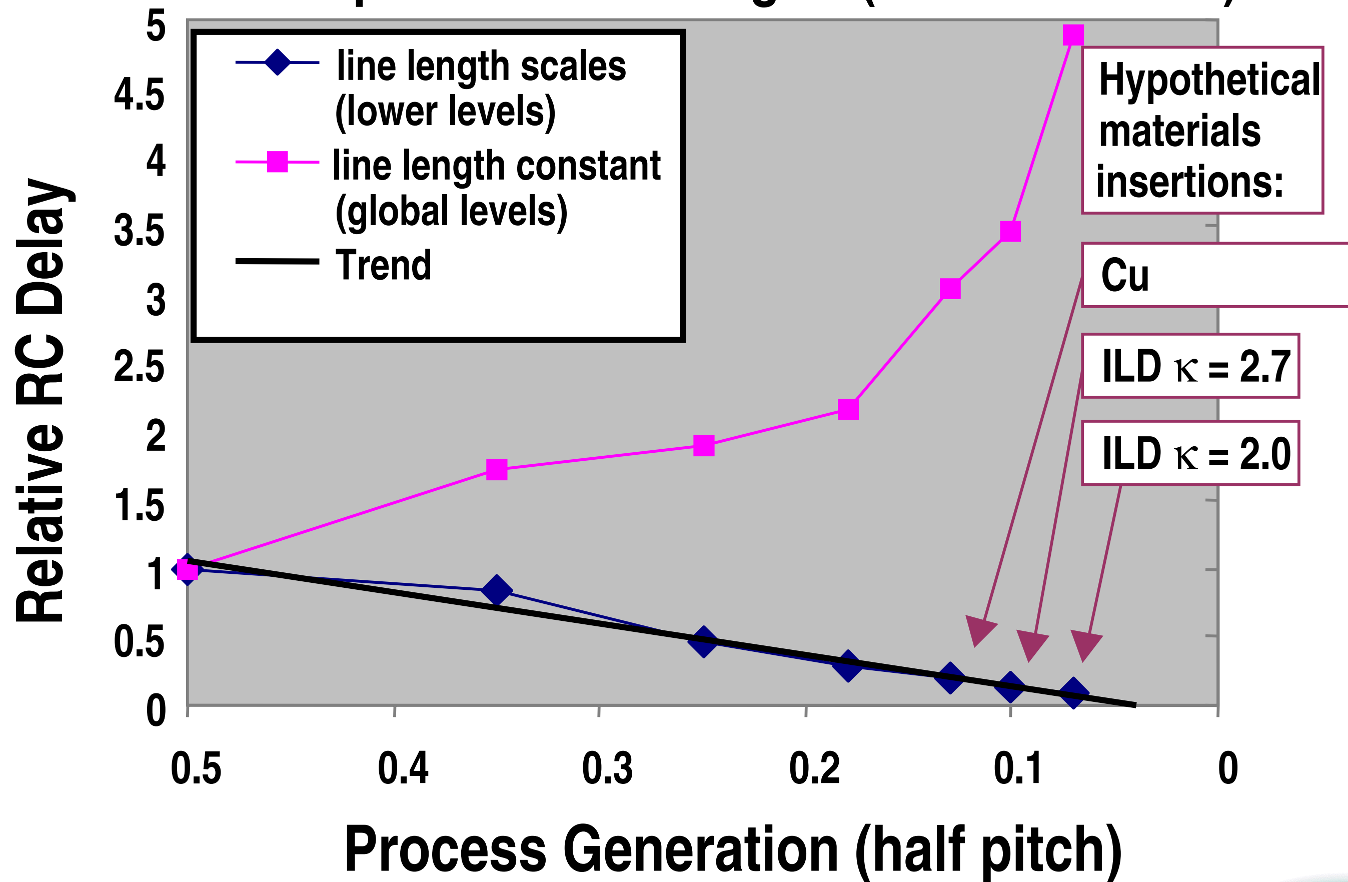
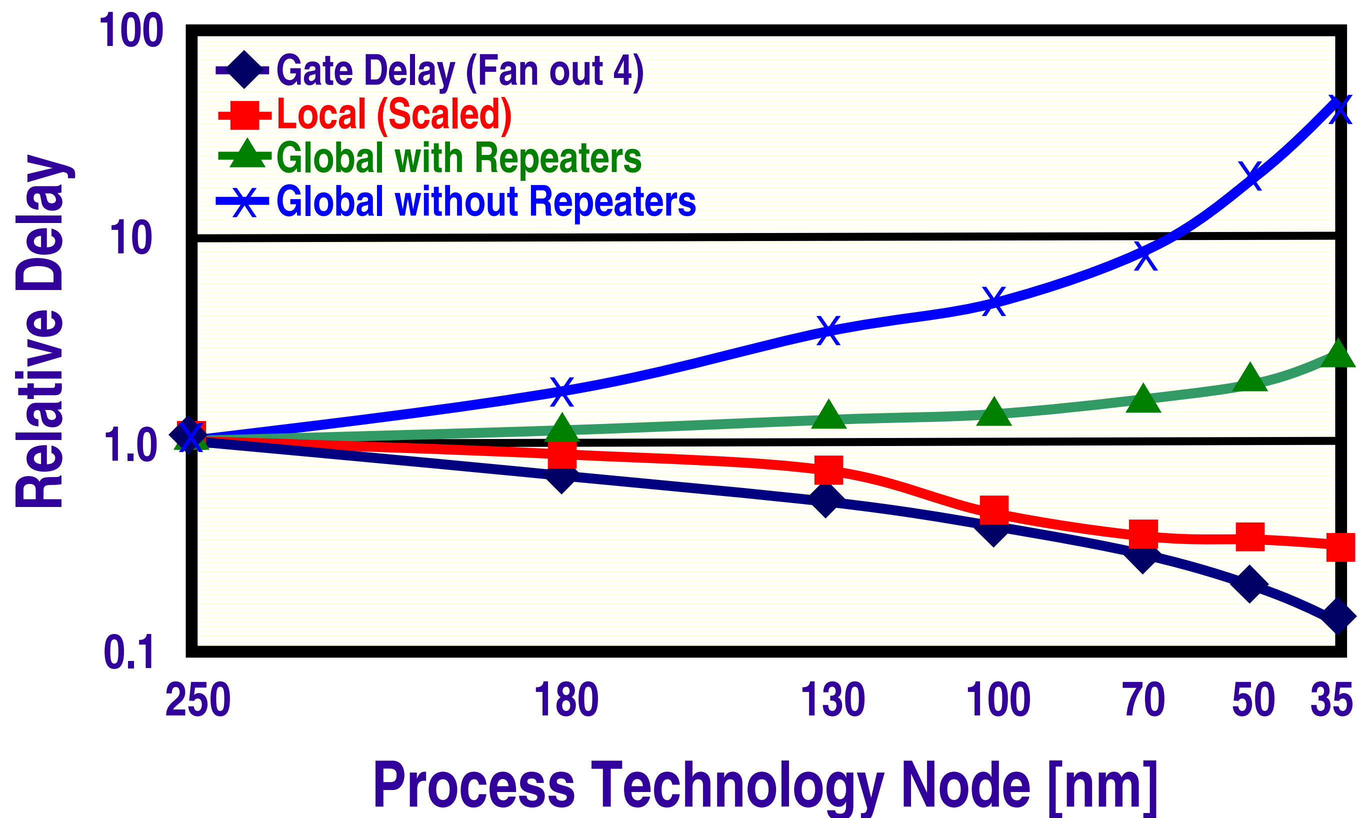
Interconnect Progression

- 1994 NTRS introduced the need for Cu and low κ materials
- 1997 NTRS describes the adoption of these materials
- 1999 ITRS highlighted
  - Rapid changes in materials
  - Materials solutions alone cannot deliver performance - end of traditional scaling in sight

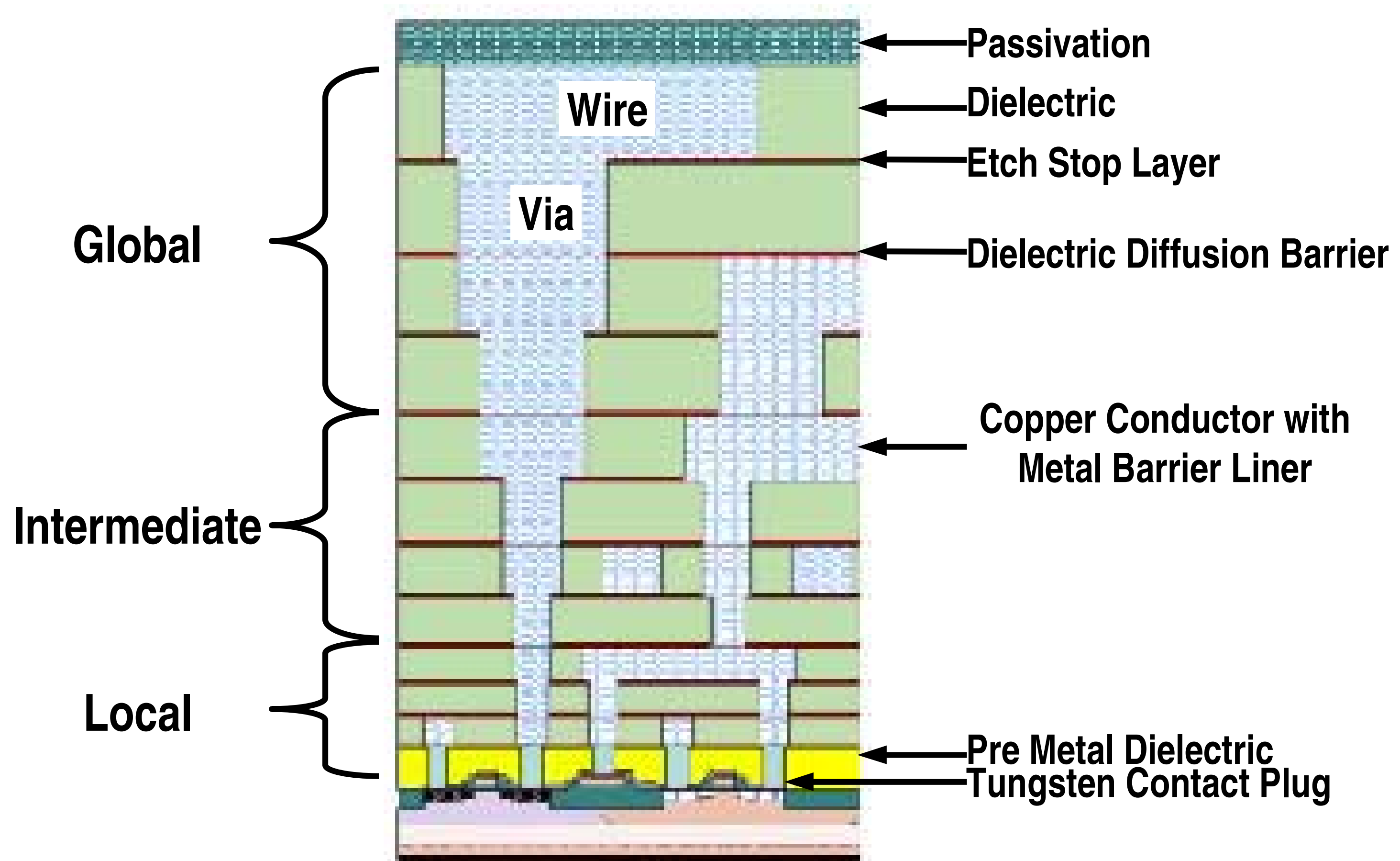
No Moore Scaling!



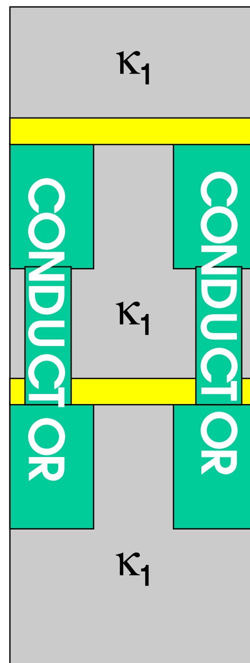
Delay for Local & Global Wiring versus Feature Size



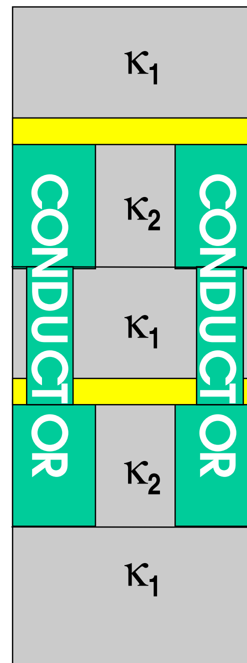
Typical Chip Cross-section of Hierarchical Scaling



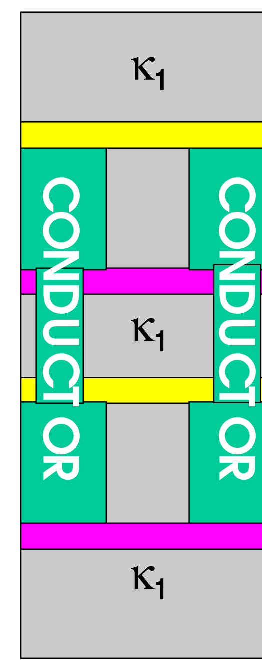
Typical ILD structures



Homogeneous ILD without trench etch stop



Embedded low κ ILD ($\kappa_1 > \kappa_2$)



Homogeneous ILD with trench etch stop

Difficult Challenges

> 100 nm

- New materials
- Reliability
- Process integration
- Dimensional control
- Interconnect process with low/no device impact

<100 nm

- Dimensional control
- Aspect ratios for fill and etch
- New materials and size effects
- Process integration
- Solutions beyond copper and low κ

Materials Challenges

- Near term
  - Rapid introduction of materials
    - new barriers and seed layers
      - in situ formed dielectric and metal
    - new dielectrics (both low and high κ)
    - ferroelectrics
  - Combination of materials and technologies
    - to address SOC needs
  - Many new reliability challenges
    - new materials and interfaces
    - electrical, thermal and mechanical exposure

Materials Challenges

- Long term
  - Continued introduction of materials
    - barriers seed layers for optical, low temp, RF, air gap
    - conducting polymers, cooled conductors, alternate metals, superconductors
  - More reliability challenges
  - Microstructural and atom scale effects

Dimensional Control

- **Multi-dimensional control of features**
  - performance and reliability implications
- **Multiple levels**
  - reduced feature size, new materials and pattern dependent processes
  - process interactions
    - CMP and deposition - dishing and erosion
    - Deposition and etch - to pattern multi-layer dielectrics
- **Aspect ratios for etch and fill**
  - particularly DRAM contacts and dual damascene

Process Integration

- Combinations and interactions of new materials and technologies
  - interfaces, contamination, adhesion, diffusion, leakage concerns, thermal budget, ESH, CoO
- Structural complexity
  - levels - interconnect, ground planes, decoupling capacitors
  - passive elements
  - other SOC interconnect design needs (RF)
  - cycle time

Solutions beyond Cu and low κ

- Material innovation combined with traditional scaling will no longer satisfy performance requirements
  - Design, packaging and interconnect innovation needed
  - What's next?
    - optical, RF, low temperature
    - novel active devices (3D or multi-level)

MPU Near Term Requirements

Year	1999	2000	2001	2002	2003	2004	2005
Technology Node	180 nm			130 nm			100 nm
MPU ½ pitch	230	210	180	160	145	130	115
MPU gate length (nm)	140	120	100	85	80	70	65
Number of metal levels	6–7	6–7	7	7–8	8	8	8–9
Number of optional levels—ground planes/capacitors	0	0	0	2	2	2	2
Jmax (A/cm^2)—wire (at 105° C)	5.80E+05	7.10E+05	8.00E+05	9.60E+05	1.10E+06	1.30E+06	1.40E+06
Imax (mA)—via (at 105° C)	0.36	0.36	0.33	0.32	0.29	0.27	0.24
Local wiring pitch (nm)	500	450	405	365	330	295	265
Local A/R (for Al)	2	2	2.1	2.1	2.2	**	**
Local A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.7
Cu local dishing (nm), 5% x height	18	16	15	14	13	12	11
Intermediate wiring pitch (nm)	640	575	520	465	420	375	340
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**
Intermediate wiring dual damascene A/R (Cu wire/via)	2.0/2.1	2.1/2.1	2.2/2.1	2.2/2.1	2.2/2.2	2.3/2.2	2.4/2.2
Cu intermediate dishing (nm), 15 micron wide wire, 10% x height	64	60	57	51	46	43	41

** This technology is not expected to extend to this node

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

MPU Near Term Requirements (contd.)

Year	1999	2000	2001	2002	2003	2004	2005
Technology Node	180 nm			130 nm			100 nm
Dielectric erosion (nm), intermediate wiring, 50% areal density, 10% x height	64	60	57	51	46	43	41
Minimum global wiring pitch (nm)	1050	945	850	765	690	620	560
Global wiring A/R (Al)	2	2.1	2.2	2.3	2.4	**	**
Global wiring dual damascene A/R (Cu wire/via)	2.2/2.4	2.3/2.6	2.4/2.7	2.5/2.7	2.6/2.8	2.7/2.8	2.7/2.8
Cu global wiring dishing (nm), 15 micron wide wire, 10% x height	116	109	102	95	90	84	76
Conductor effective resistivity (mW-cm) Al wiring	3.3	3.3	3.3	3.3	3.3	**	**
Conductor effective resistivity (mW-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (for Cu wiring) (nm)***	17	16	14	13	12	11	10
Interlevel metal insulator —effective dielectric constant (κ)	3.5—4.0	3.5—4.0	2.7—3.5	2.7—3.5	2.2—2.7	2.2—2.7	1.6—2.2

* Assumes a conformal barrier/nucleation layer

** This technology is not expected to extend to this node

*** Calculated for a conformal layer in local wiring to meet minimum effective conductor resistivity

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

MPU Near Term Requirements

- 8 levels of metal
- Possible additional levels for ground planes and decoupling capacitors
- Cu adopted from 180 nm - performance is driver
- Cu A/R reduced compared to Al for capacitance reduction

MPU Near Term Requirements (contd)

- Hierarchical wiring methodology is followed in the MPU
  - Pitch and metal thickness adjusted at each level
- New planarization dishing and erosion requirements to ensure performance targets are achieved
- Conformal barriers are specified with decreasing thickness requirements tied to achieving specified resistivity targets
- Effective κ relaxed (*vs* 97 NTRS) reflecting benefit of lower A/R Cu wires resulting in reduced capacitance

MPU Long Term Requirements

Year	2008	2011	2014
Technology Node	70 nm	50 nm	35 nm
MPU ½ pitch	80	55	40
MPU gate length (nm)	45	32	22
Number of metal levels	9	9–10	10
Number of optional levels – ground planes/capacitors	3	4	4
Jmax (A/cm^2)—wire (at 105°C)	2.10E+06	3.70E+06	4.60E+06
Imax (mA)—via (at 105°C)	0.18	0.16	0.11
Local wiring pitch (nm)	185	130	95
Local A/R (for Cu)	1.9	2.1	2.3

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

MPU Long Term Requirements (contd.)

Year	*2008*	*2011*	*2014*
Technology Node	*70 nm*	*50 nm*	*35 nm*
Intermediate wiring pitch (nm)	240	165	115
Intermediate wiring dual damascene A/R (Cu wire/via)	2.5/2.3	2.7/2.4	2.9/2.5
Cu intermediate wiring dishing (nm), 15 micron wide wire, 10% x height	30	22	17
Dielectric erosion (nm), intermediate wiring	0	0	0
Minimum global wiring pitch (nm)	390	275	190
Global wiring dual damascene A/R (Cu wire/via)	2.8/2.9	2.9/3.0	3.0/3.1
Cu global wiring dishing (nm), 15 micron wide wire, 10% x height	55	38	29
Conductor effective resistivity ($\mu\Omega$-cm) Cu wiring	1.8	< 1.8	< 1.8
Barrier/cladding thickness (nm)	0	0	0
Interlevel metal insulator— effective dielectric constant (κ)	1.5	< 1.5	< 1.5

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

MPU Long Term Requirements

- Dielectric erosion must be reduced to zero to achieve performance targets
- Cu interconnect resistivity will require a zero barrier thickness
  - barrier-free deposition
  - *in situ* formed metal or dielectric barriers
- Effective κ less than 1.5 have No Known Solutions

DRAM Near Term Requirements

Up to 4 interconnect levels

Year	1999	2000	2001	2002	2003	2004	2005
Technology Node	180 nm			130 nm			100 nm
DRAM ½ pitch	180	165	150	130	120	110	100
Number of metal levels	3	3	3	3–4	4	4	4
Contact A/R—stacked capacitor	9.3	10	10.7	11.4	11.9	12.4	13
Local wiring pitch (nm) noncontacted	360	330	300	260	240	210	200
Specific contact resistance (Ω-cm^2)	3.00E-07	2.50E-07	2.00E-07	1.70E-07	1.60E-07	1.10E-07	1.00E-07
Specific via resistance (Ω-cm^2)	7.00E-09	5.00E-09	3.00E-09	2.00E-09	2.00E-09	1.00E-09	1.00E-09
Conductor effective resistivity ($\mu\Omega$-cm)*	3.3	3.3	3.3	3.3	3.3	3.3	2.2
Interlevel metal insulator—effective dielectric constant (κ)	4.1	4.1	4.1	3.0–4.1	3.0–4.1	3.0–4.1	2.5–3.0

* Assumes a conformal barrier/nucleation layer

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

DRAM Near Term Requirements

- Up to 4 interconnect levels
- Most aggressive local pitch - 200 nm @ 100 nm node (defect sensitive) and highest A/R (13.0 @ 100 nm) features of the three product classes
- Requirements for specific via and contact resistance
- Low κ required at 130 nm for high speed RAMBUS
- Cu required by 100 nm for performance although cost factors may delay introduction

DRAM Long Term Requirements

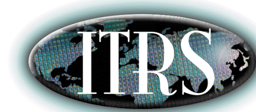
Year	*2008*	*2011*	*2014*
Technology Node	*70 nm*	*50 nm*	*35 nm*
DRAM ½ pitch	70	50	35
Number of metal levels	4	4	4
Contact A/R—stacked capacitor	14.1	16.1	23.1
Local wiring pitch (nm) non-contacted	140	100	70
Specific contact resistance (Ω-cm^2)	5.00E-08	2.50E-08	1.50E-08
Specific via resistance (Ω-cm^2)	6.00E-10	3.00E-10	1.50E-10
Conductor effective resistivity ($\mu\Omega$-cm)*	2.2	2.2	2.2
Interlevel metal insulator — effective dielectric constant (κ)	2.5–3.0	2.0–2.5	2.0–2.3

* Assumes a conformal barrier/nucleation layer

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

No Known Solutions to A/R

High κ materials may provide some relief



SOC Near Term Requirements

Year	1999	2000	2001	2002	2003	2004	2005
Technology Node	180 nm			130 nm			100 nm
MPU ½ pitch (nm)	230	210	180	160	145	130	115
ASIC gate (nm)	180	165	150	130	120	110	100
Number of metal levels	6	6	7	7	7–8	8	8
Number of optional levels—passive elements	1	1	2	2	4	4	4
Local wiring pitch (nm)	450	405	360	325	290	260	230
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2	**	**
Local wiring A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.7
Intermediate wiring pitch (nm)	560	505	450	405	360	325	285
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**

** This technology is not expected to extend to this node

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

SOC characterized by more aggressive local pitch than MPU.

Passive elements require the use of more levels of metal.

SOC Near Term Requirements (contd.)

Year	1999	2000	2001	2002	2003	2004	2005
Technology Node	180 nm			130 nm			100 nm
Intermediate via A/R (Al)	2.8	2.8	2.9	2.9	3	**	**
Intermediate wiring dual damascene A/R (Cu wire/via)	2.0/2.1	2.1/2.1	2.2/2.1	2.2/2.1	2.2/2.2	2.3/2.2	2.4/2.2
Global wiring pitch (nm)	900	810	720	650	580	520	460
Global wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**
Global wiring dual damascene A/R (Cu wire/via)	2.2/2.4	2.3/2.6	2.4/2.7	2.5/2.7	2.6/2.8	2.7/2.8	2.7/2.8
Interlevel metal insulator—effective dielectric constant (κ)	3.5–4.0	3.5–4.0	2.7–3.5	2.7–3.5	2.2–2.7	2.2–2.7	1.6–2.2

** This technology is not expected to extend to this node

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

SOC Near Term Requirements

– **SOC characterized by more aggressive local pitch than MPU**

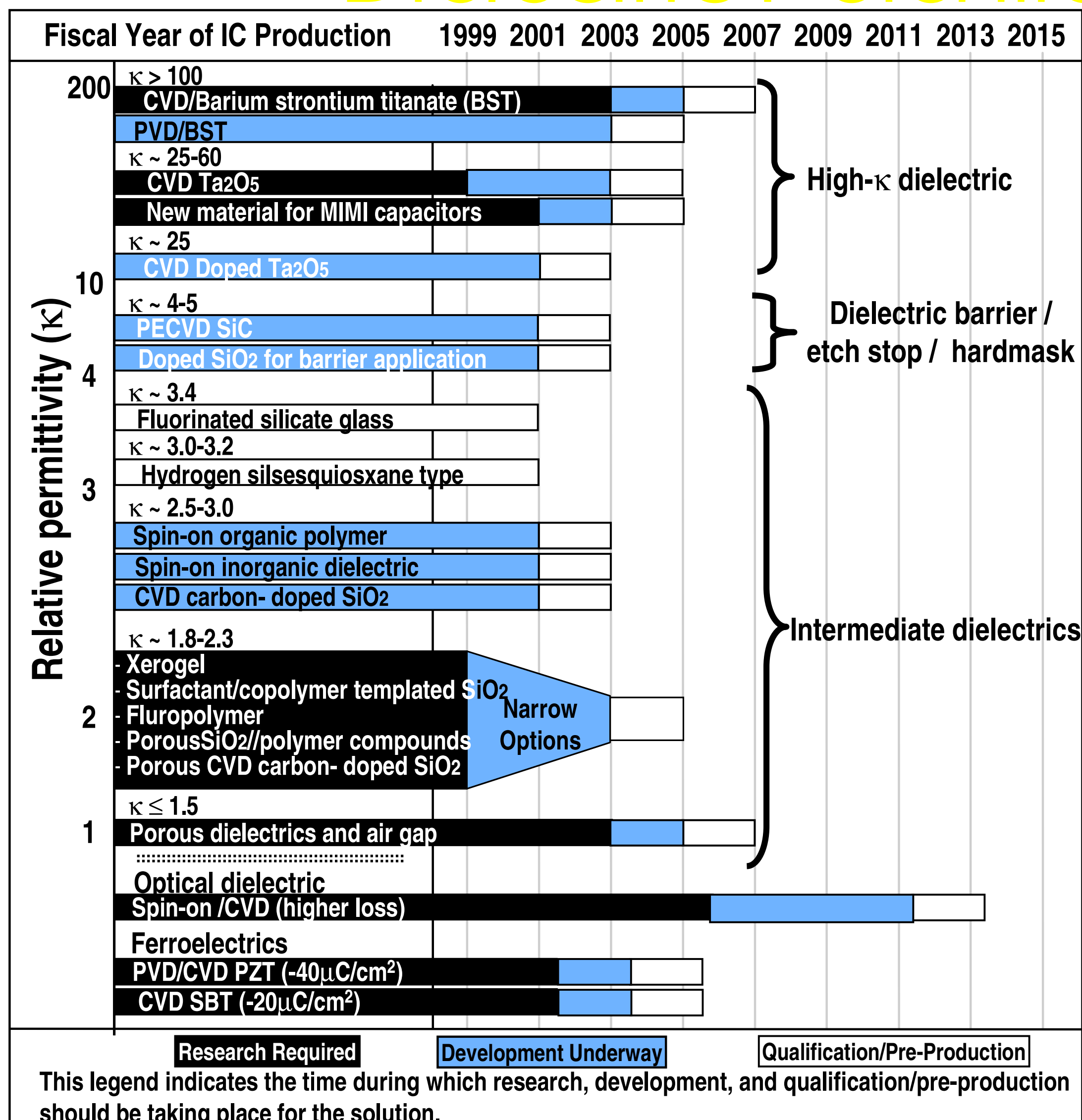
– **Passive elements require the use of more levels of metal**

SOC Long Term Requirements

Year	2008	2011	2014
Technology Node	70 nm	50 nm	35 nm
MPU ½ pitch (nm)	80	55	40
ASIC gate (nm)	70	50	35
Number of metal levels	9	9–10	10
Number of optional levels—passive elements	6	6	6
Local wiring pitch (nm)	165	120	85
Local wiring A/R (for Cu)	1.9	2.1	2.2
Intermediate wiring pitch (nm)	210	145	110
Intermediate wiring dual damascene A/R (Cu wire/via)	2.5/2.3	2.7/2.4	2.9/2.5
Global wiring pitch (nm)	330	240	170
Global wiring dual damascene A/R (Cu wire/via)	2.8/2.9	2.9/3.0	3.0/3.1
Interlevel metal insulator—effective dielectric constant (κ)	1.5	< 1.5	< 1.5

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

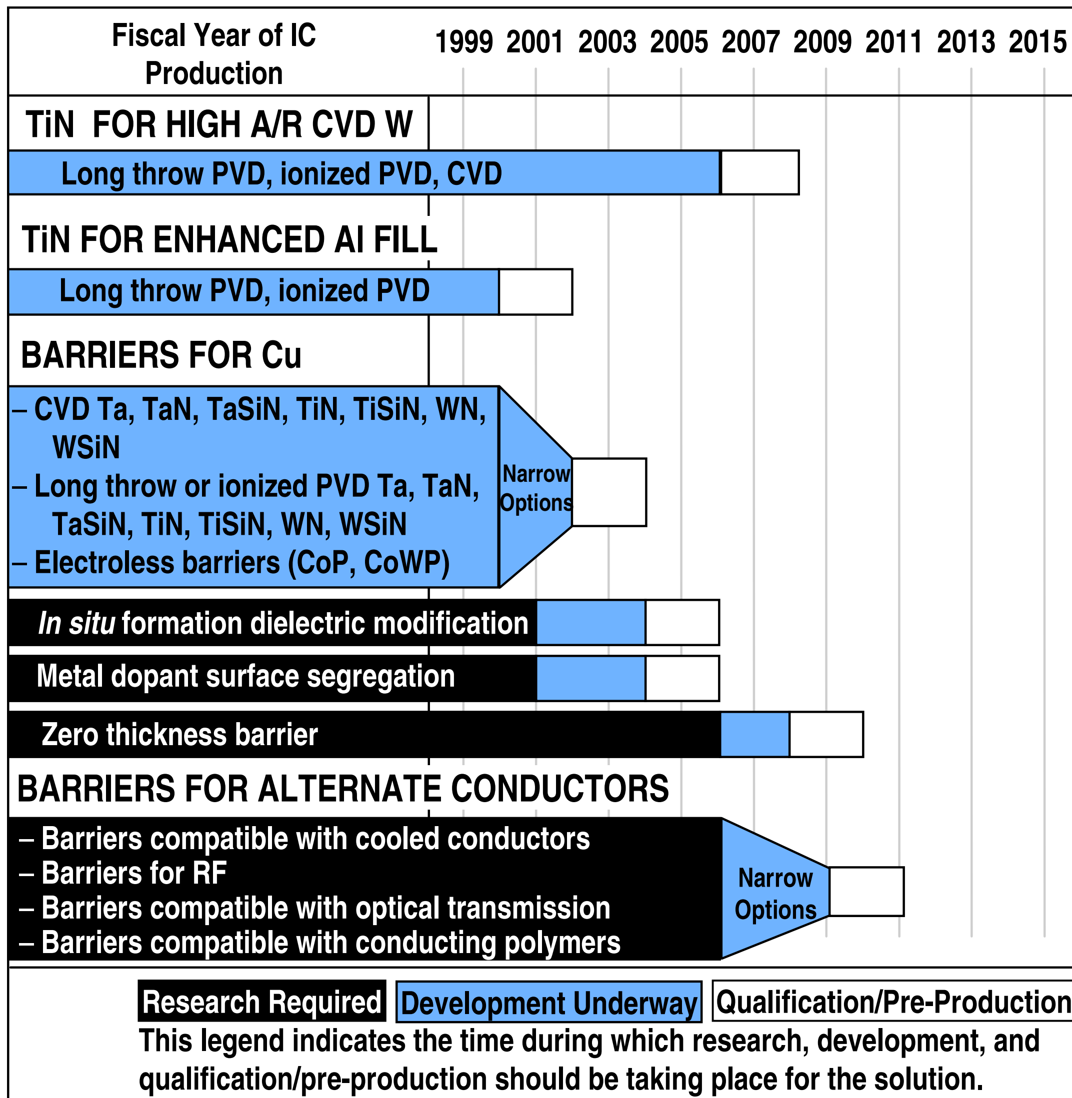
Dielectric Potential Solutions



Challenges

- High κ and ferroelectrics materials development
- Development and integration of ultra low κ materials with acceptable mechanical/thermal properties
- Fabricating low-temp low-loss SiO_2 optical interconnect
- Addressing turning radius of higher loss polymer optics

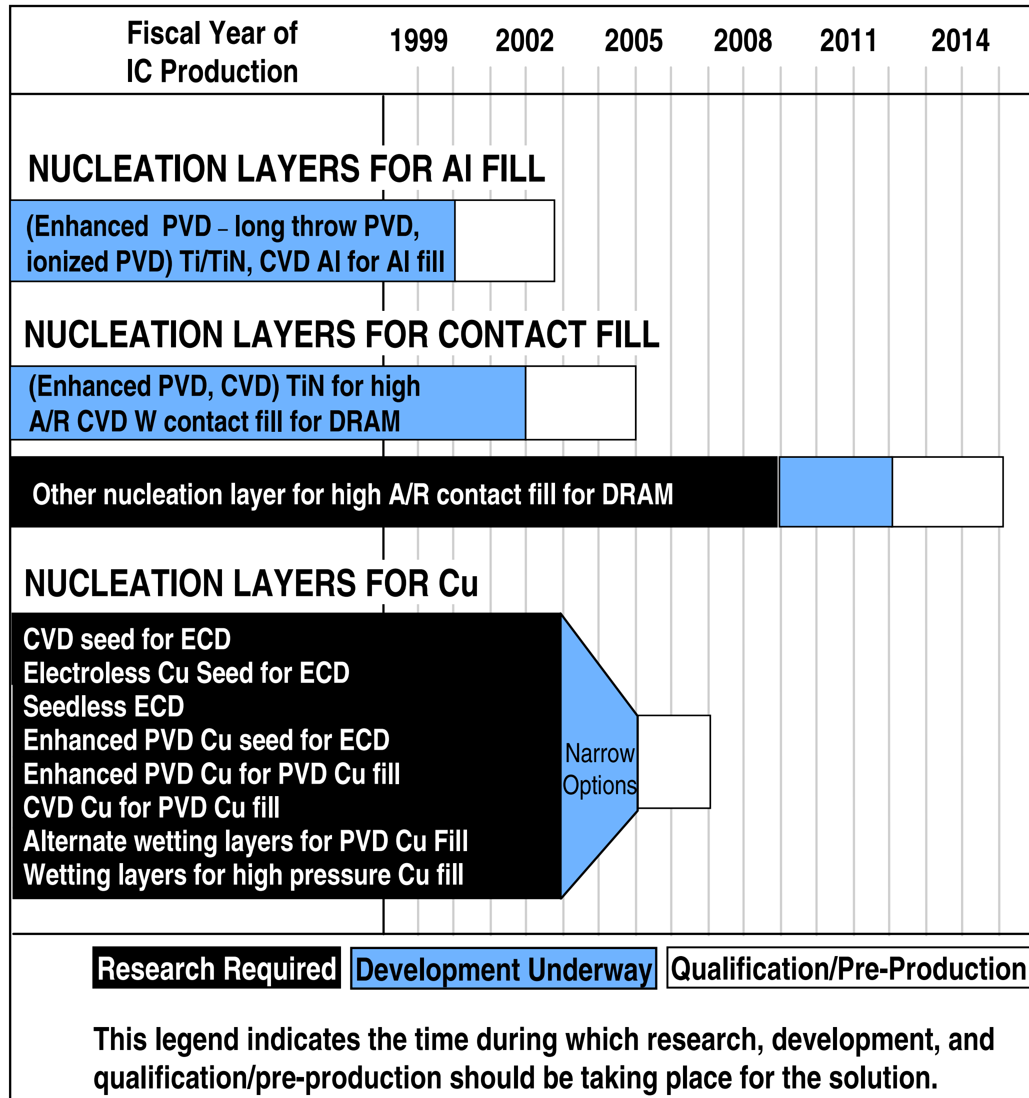
Barrier Potential Solutions



Challenges

- Solutions for high A/R DRAM contacts
- Conformal barriers for dual damascene Cu - thin, effective diffusion barrier, low via resistance
- Barrier free solutions to reduce effective Cu resistivity

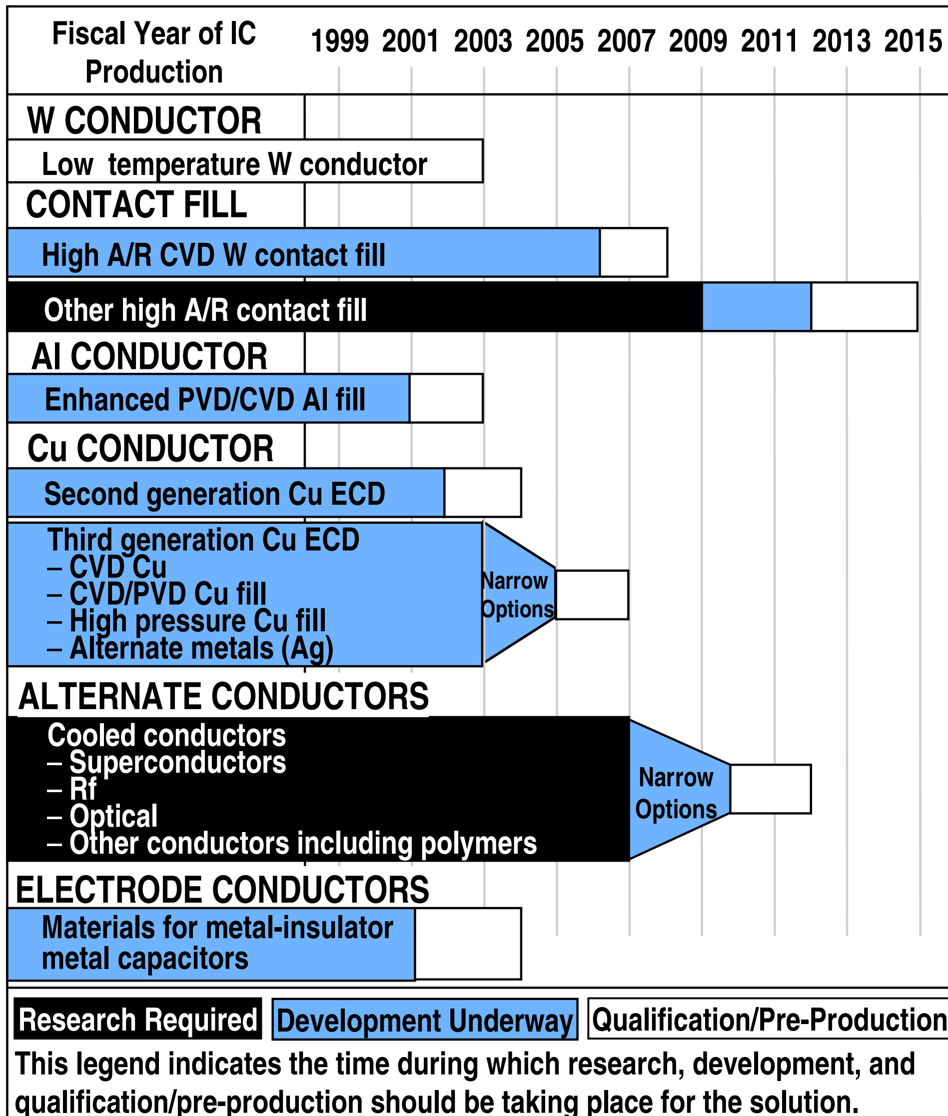
Nucleation Potential Solutions



Challenges

- Solutions for high A/R Al vias
- Nucleation layers other than TiN for high A/R DRAM contacts
- Advanced nucleation layers for Cu interconnect which do not degrade conductor effective resistivity

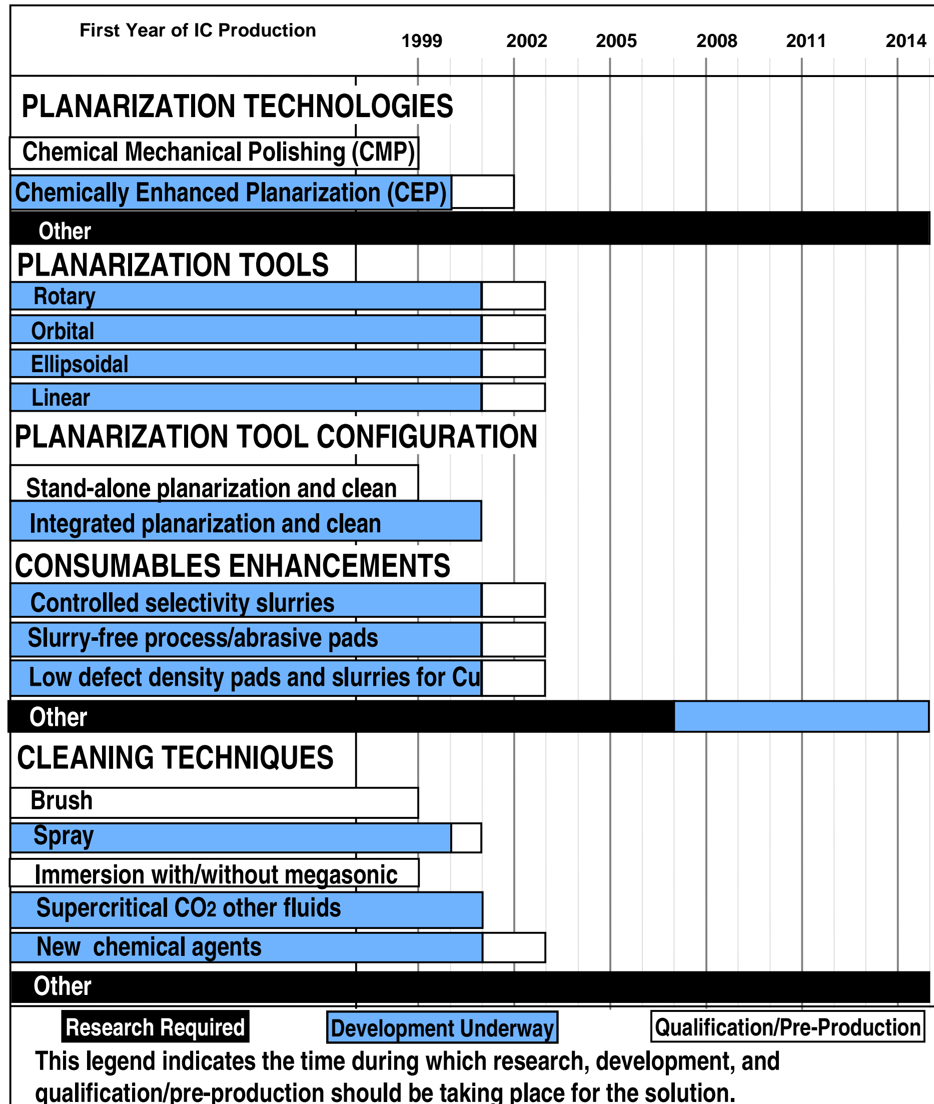
Conductor Potential Solutions



Challenges

- Low temp CVD W for low κ compatibility
- High A/R contact fill for DRAM
- Cu fill of dual damascene structures with reduced CD and high A/R
- Identifying and implementing solutions after Cu and low κ

Planarization Potential Solutions



Challenges

Continued development of tools/slurries/pads

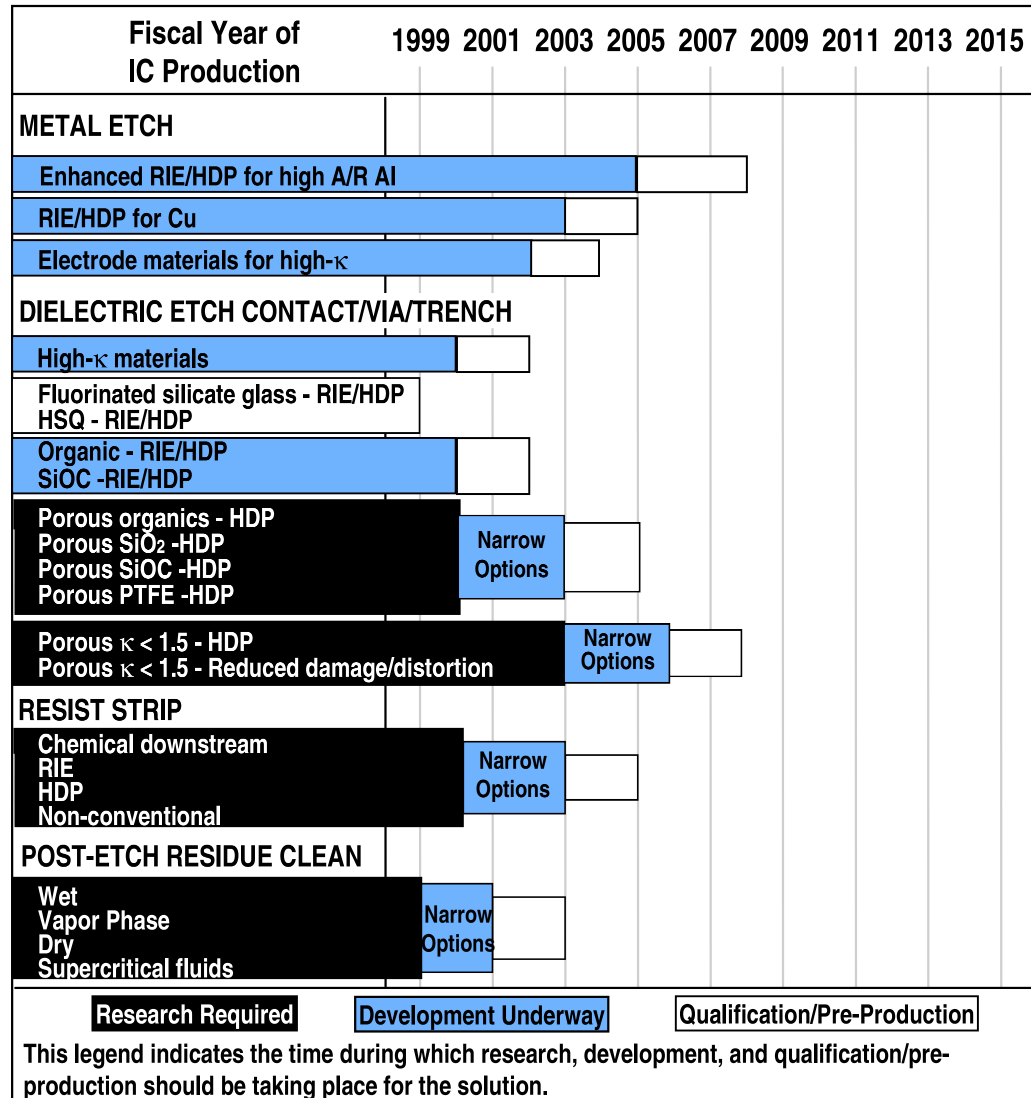
Cleaning technologies

Many new low and high κ materials - may require new planariztion approaches

Pattern dependent planarization

Planarization over passive elements for SOC

Etch Potential Solutions



Challenges

- Dimensional control with small features and high A/R
- Selectivity to etch stops and hard masks
- Many new low and high κ materials - may require new chemistries
- Strip/clean compatibility with these new materials
- Low damage

Long Term Prospective

- Cu/low κ interconnects extendable for local/intermediate wiring
  - Crosstalk must be carefully managed
  - Dimensional effects at < 50 nm may raise effective resistivity of conductor

Long Term Prospective (contd)

- Global wiring is problem
  - Design solutions with repeaters, new architectures - helps
  - Coplanar waveguides and free space RF provide
    - High bandwidth
    - Low frequency dispersion and low loss
    - Modular interconnect including compatibility with traditional on-chip and off-chip interconnect technologies
  - Optical interconnects add
    - No frequency-dependent loss or crosstalk
    - No distance-dependent loss or degradation

Last words

- Rapid changes in materials
- Materials solutions alone cannot deliver performance - end of traditional scaling
- System level solutions must be accelerated
- System on a Chip implementations will propagate
- SOC may change competitive picture - functionality not cost/area
- Optical/rf/waveguide/3D current alternatives