

ORTC -
ITRS 1999 Table Status Review
ITRS Conference - S.Clara, CA
7/8,9

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International Technology Roadmap for Semiconductors



Agenda

- 1999 ITRS ORTC Table Proposal Review
- Focus Topic Analysis
 - ITRS Node
 - Chip Size Model Status
 - Function Density
 - Chip Frequency
 - Affordable Cost
- Summary / Plans

1999 ITRS ORTC Table Proposal Review

- Table 1 - Technology Generations
- Table 2 - Chip Size
- Table 3 - Performance and Packaged Chips
- Table 4 - Electrical Defects
- Table 5 - Power Supply and Dissipation
- Table 6 - Cost

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ITRS Technology Node Update

- *Key Node Indicators:*
 - *DRAM Half-Pitch*
 - *MPU Isolated Line (Printed Gate Length)*
- *Historical: Both on 2-Year Cycle (70% Reduction)*
 - *1995 -> 1997 -> 1999*

Source: *!! WORK IN PROGRESS !!* * 4/13 Munich ITWG/IRC Consensus

ITRS Technology Node Update (cont.)

- ITRS Forecast Period 1999-2014:
 - DRAM, MPU Half-Pitch (180nm DRAM/1999, 230nm MPU/1999):
 - 3-year Cycle after 1999* (*1-year pull-in? - Not in the 1999 Roadmap*)
 - MPU Isolated Line (Printed Gate Length) (140nm/1999):
 - one more 2-year Cycle, then
 - projecting 3-year Cycle after 2001*

Source: *!! WORK IN PROGRESS !!* * 4/13 Munich ITWG/IRC Consensus

4/13/99 ITWG/IRC Meeting Technology Node Proposal Header Format :

SHORT TERM YEARS

<i>YEAR OF INTRODUCTION "TECHNOLOGY NODE"</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>	<i>DRIVER</i>
<i>DRAM ½ PITCH (nm)</i>	<i>180</i>	<i>165</i>	<i>150</i>	<i>130</i>	<i>120</i>	<i>110</i>	<i>100</i>	<i>D ½</i>
<i>MPU GATE LENGTH (nm)</i>	<i>140</i>	<i>120</i>	<i>100</i>	<i>85</i>	<i>80</i>	<i>70</i>	<i>65</i>	<i>M GATE</i>
<i>MPU / ASIC ½ PITCH (nm)</i>	<i>230</i>	<i>210</i>	<i>180</i>	<i>160</i>	<i>145</i>	<i>130</i>	<i>115</i>	<i>M & A ½</i>
<i>ASIC GATE LENGTH (nm)</i>	<i>180</i>	<i>165</i>	<i>150</i>	<i>130</i>	<i>120</i>	<i>110</i>	<i>100</i>	<i>A GATE</i>

LONG TERM YEARS

<i>YEAR OF INTRODUCTION "TECHNOLOGY NODE"</i>	<i>2008 70 nm</i>	<i>2011 50 nm</i>	<i>2014 35 nm</i>	<i>DRIVER</i>
<i>DRAM ½ PITCH (nm)</i>	<i>70</i>	<i>50</i>	<i>35</i>	<i>D ½</i>
<i>MPU GATE LENGTH (nm)</i>	<i>45</i>	<i>32</i>	<i>22</i>	<i>M GATE</i>
<i>MPU / ASIC ½ PITCH (nm)</i>	<i>80</i>	<i>55</i>	<i>40</i>	<i>M & A ½</i>
<i>ASIC GATE LENGTH (nm)</i>	<i>70</i>	<i>50</i>	<i>35</i>	<i>A GATE</i>

Source: **!! WORK IN PROGRESS !!** 4/13 Munich ITWG/IRC Consensus

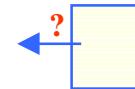
4/13/99 ITWG/IRC Meeting Technology Node Proposal Status

Summary Plus Analysis (update 6/2):

Technology Node (nm) "Agreement in Principle" as of 4/13/99 Munich ITWG/IRC Meeting:																	CAGR '99-'05	CAGR '05-'14	
Year	1999 180nm	2000	2001	2002 130nm	2003	2004	2005 130nm	2006	2007	2008 70nm	2009	2010	2011 50nm	2012	2013	2014 35nm	DRIVER		
DRAM Half-Pitch (DHP)	180	165	150	130	120	110	100	89	79	70	63	56	50	44	39	35	DRAM	-9.3%	-10.3%
MPU Gate Length (MGL)	140	120	100	85	80	70	65	58	51	45	40	36	32	28	25	22	MPU	-12.0%	-11.6%
MPU/ASIC Half-Pitch (MAHP)	230	210	180	160	145	130	115	102	90	80	71	62	55	49	44	40	MPU & ASIC	-10.9%	-11.0%
ASIC Gate Length (AGL)	180	165	150	130	120	110	100	89	79	70	63	56	50	44	39	35	ASIC	-9.3%	-10.3%
Ratio to DRAM Half-Pitch:																			
DRAM HP	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00			
MPU GL	0.78	0.73	0.67	0.65	0.67	0.64	0.65	0.65	0.65	0.64	0.64	0.64	0.64	0.64	0.63	0.63			
M/A HP	1.28	1.27	1.20	1.23	1.21	1.18	1.15	1.15	1.15	1.14	1.13	1.11	1.10	1.11	1.13	1.14			
ASIC GL	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00			
Note: 1) Numbers through 2005 are the annualized "rounded" numbers negotiated between the IRC and the Litho TWG.																			
2) The three-year technology nodes after 2005 (2008, 2011, 2014) are 3-year cycle (~.5x / every other cycle).																			
3) Inter-node numbers after 2005 are interpolated between nodes, rounded in excel to the nearest significant figure.																			
4) The fundamental ratios starting with the 2002 node are: a) MHP/DHP = 1.15x; b) MIL/DHP = .65x																			
5) The ratio analysis table shows the effect of negotiation, rounding, and interpolation on the fundamental ratios..																			

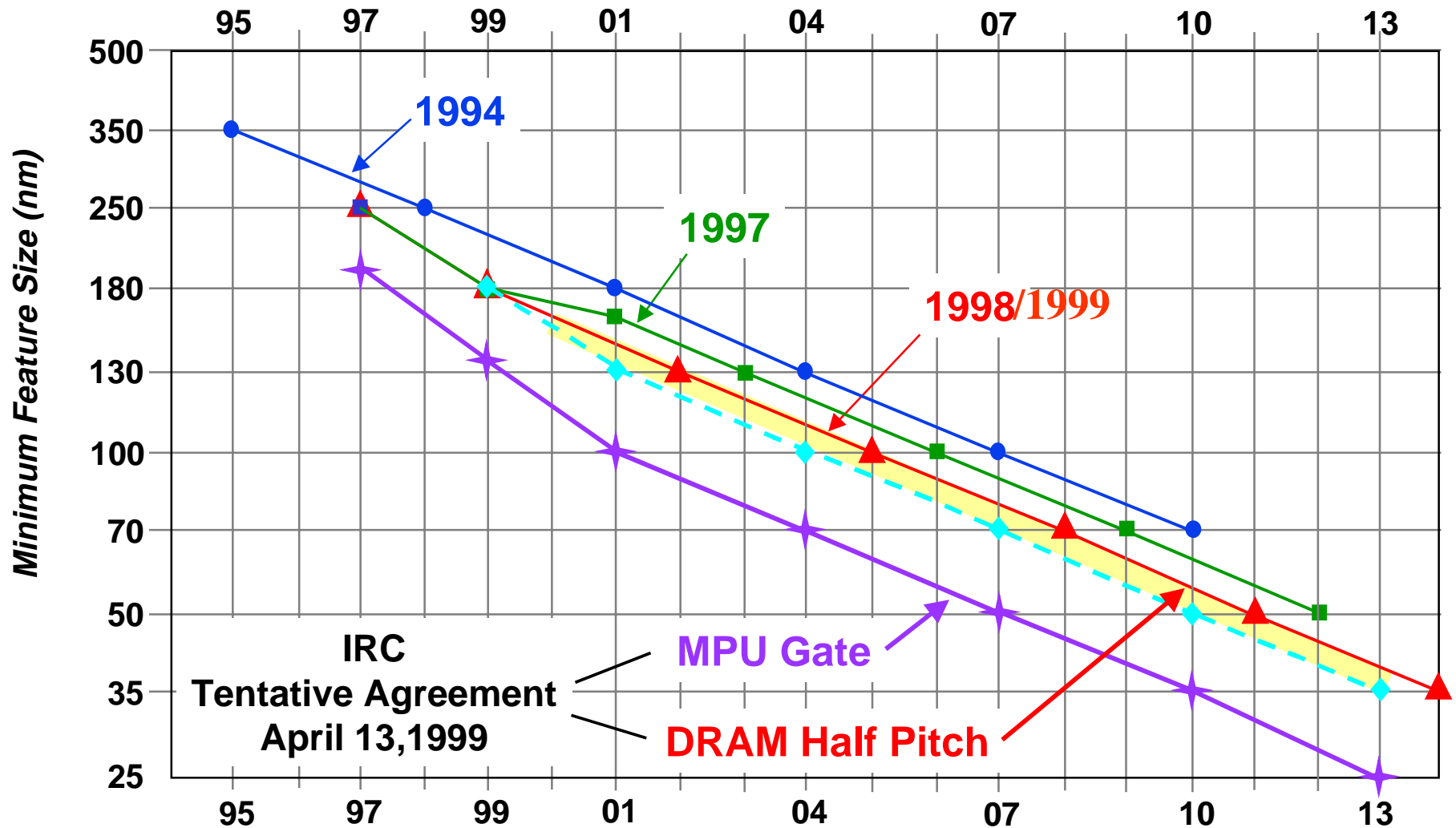
Source: *!! WORK IN PROGRESS !!* 4/13 Munich ITWG/IRC Consensus

Possible Acceleration

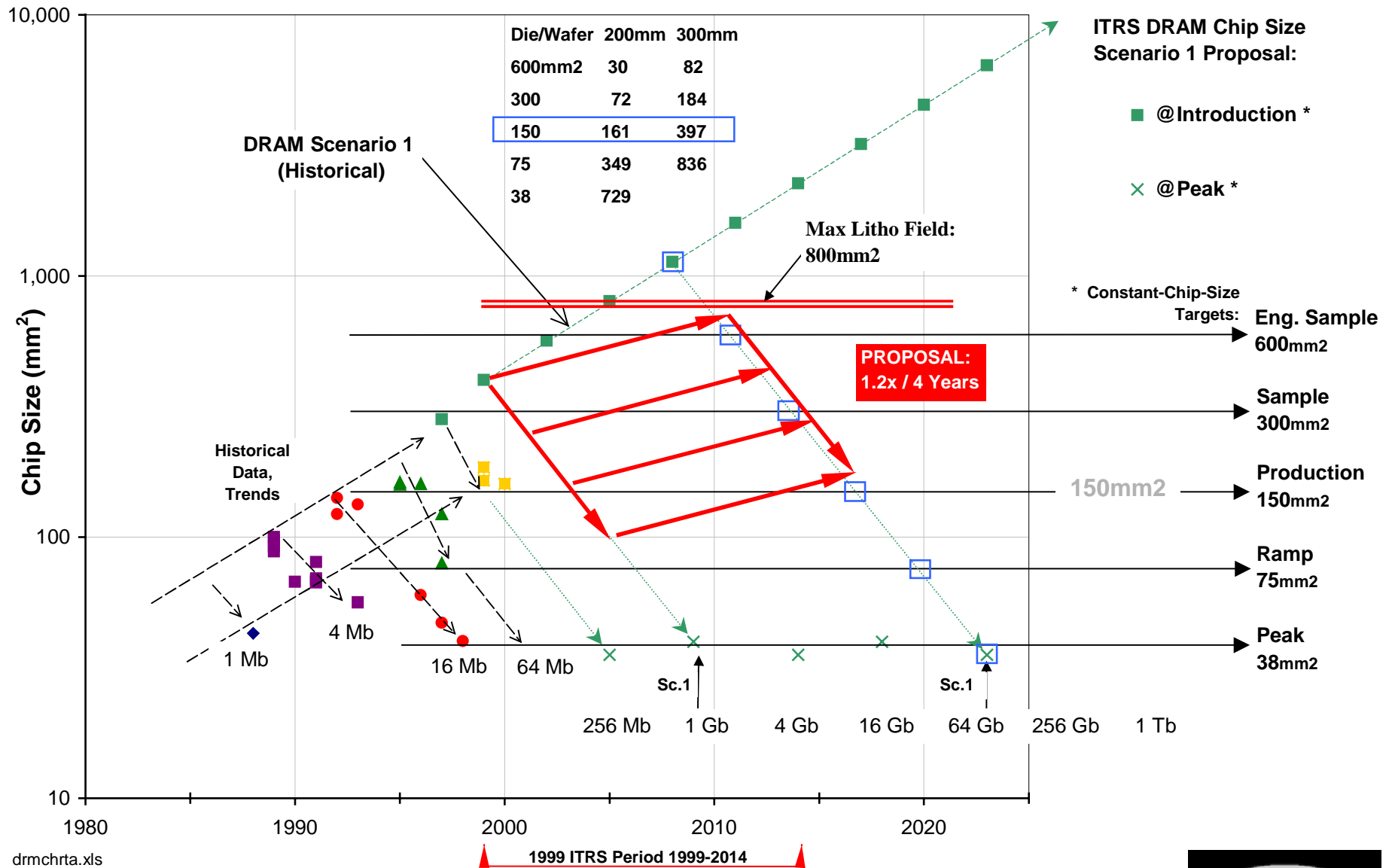


SIA Roadmap Acceleration Analysis

(from Litho TWG Summary)



Chip size: DRAM - 1999 ITRS Proposal

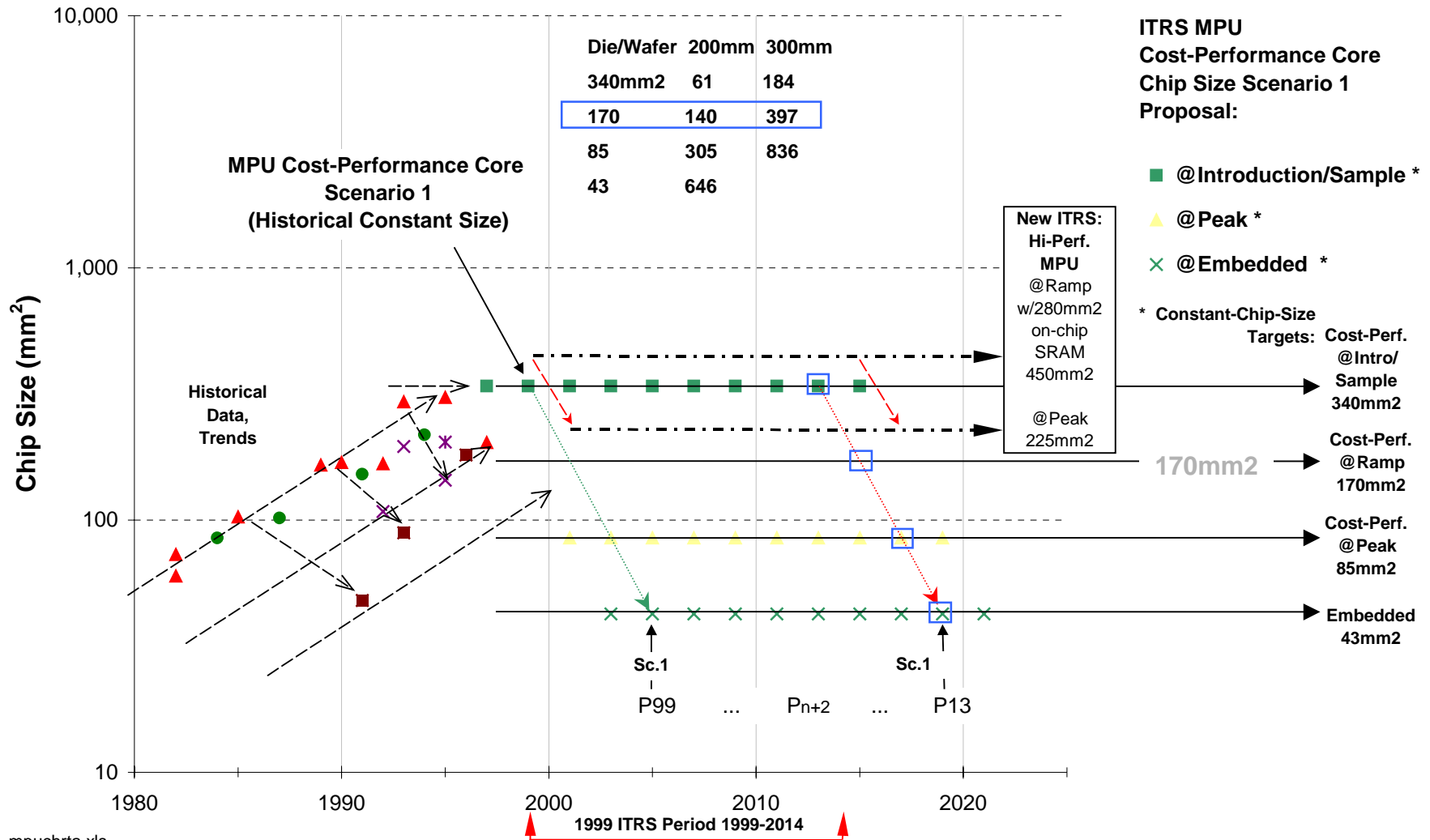


drmchrta.xls

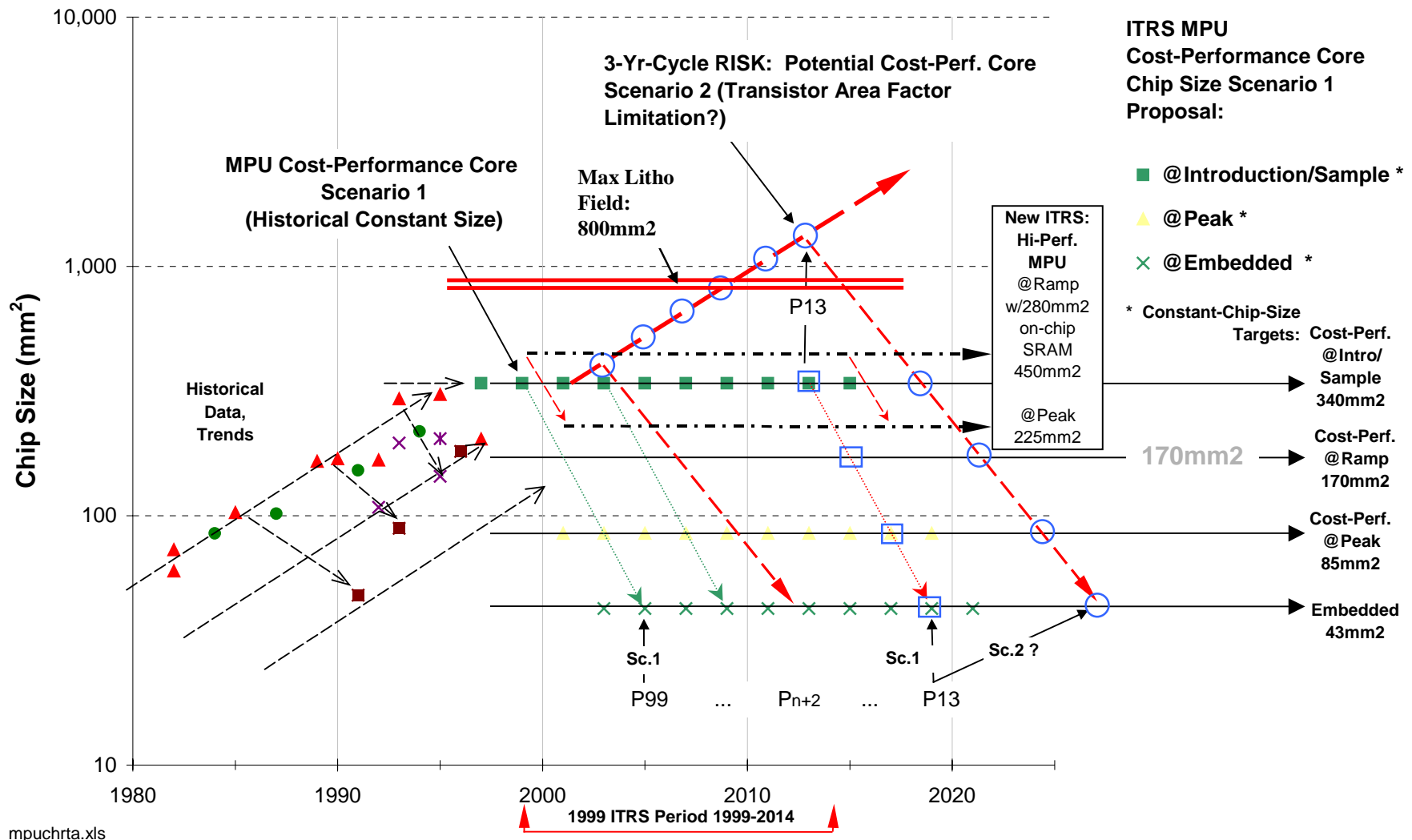
DRAM Chip size: 1999 ITRS Proposal

- *DRAM 3-Year Technology Nodes after 1999 - implies:*
 - *Return to Historical ISSC-Intro Chip Size Increase (2x / 6 Years)*
 - *.5x / 3 years litho-only InTRA-generation fundamental shrink rate*
- *Proposal 1 (IRC rejected): DRAM Constant Production Chip Size Target: 150mm² between Product Generations*
 - *Too much delay (5-6 years) between Product Generations*
- *Proposal 2 (IRC accepted 7/7) : 1.2x / 4 years Chip Size Increase per 4x Product Generation (1.1x / 2 years per 2x Product Generation)*
 - *InTRA- generation shrink rate: .25x / 6 years (.5x / 3 years, .63x / 2 years)*
 - *Risk: Requires Aggressive Design Cell-factor Improvement*

Chip size: MPU - 1999 ITRS Proposal (Scenario 1)



Chip size: MPU - 1999 ITRS Proposal (w/Potential Scenario 2)



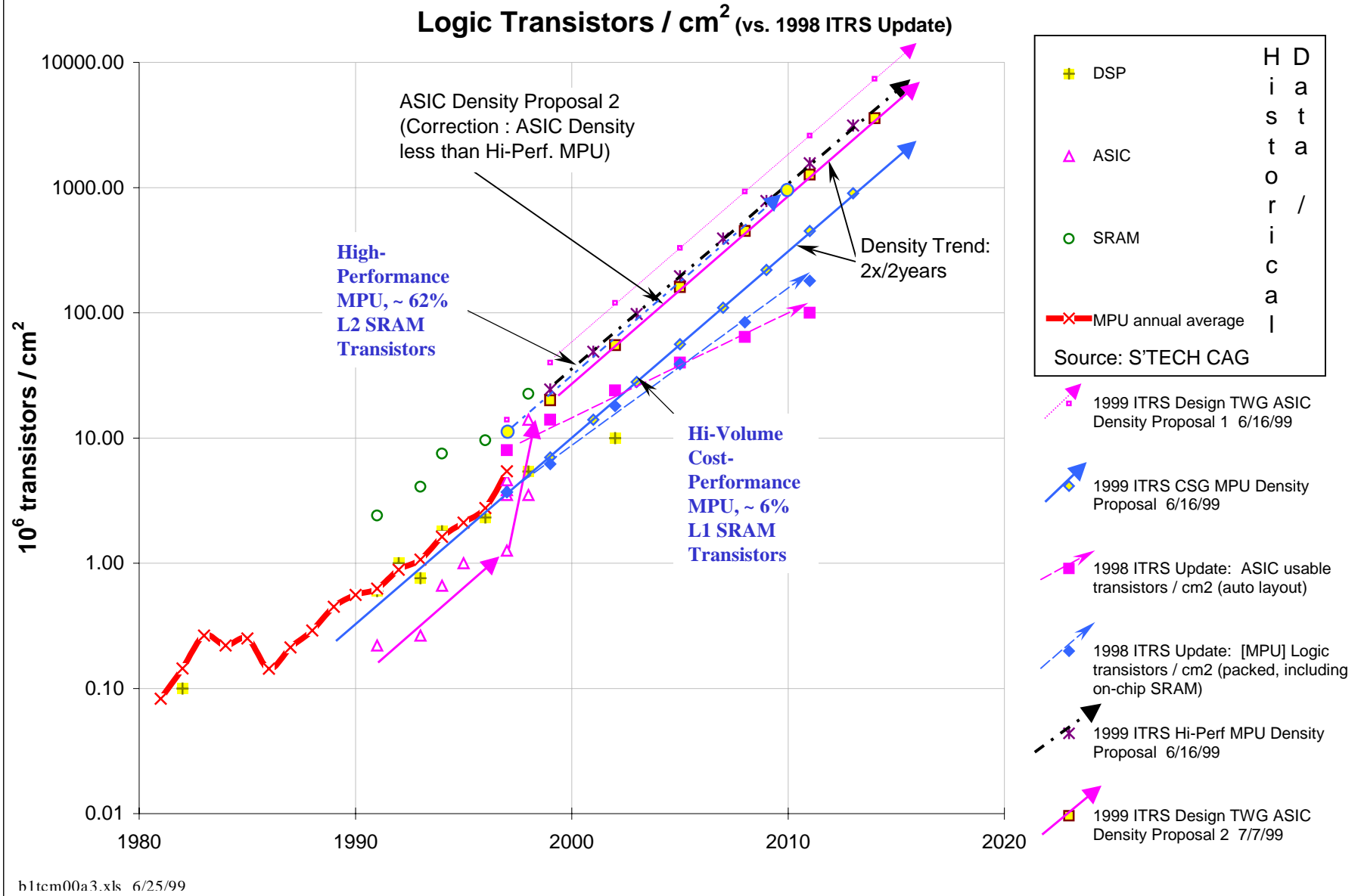
Chip size: MPU-1999 ITRS Proposal

- MPU Chip Size Proposal Similar to DRAM:
 - Projecting Constant Ramp Chip Size Target: 170mm² between Product Generations
 - (also: 340mm² Intro/Sample, 85mm²/Peak, 43mm²/Embedded)
 - Additional Assumptions:
 - **Recent Historical Introduction Chip Size Constant (Scenario 1)**
 - 2-Year Gate-Length Technology Nodes Thru 2001
 - Back to 3-year cycle after 2001
 - **2x transistors/chip 2-year period (Market Need-Moore's Law)**
 - => 2x Density increase every 2 years (Moore's Law @ constant size)
 - Shrink InTRA-Generation (constant-transistor) .5x / node period
 - **High Performance MPU adds 280mm² SRAM to Ramp-Level Core (2Mbyte/1999)**

Chip size: MPU-1999 ITRS Proposal (cont.)

- Maintaining Constant Chip Size Target more difficult if return to 3-Year Cycle
 - ***Potential Transistor Area Factor Design Limitation Similar to DRAM Cell Factor Design Limitations? (Scenario 2?)***
 - Especially after 2001 - starting 3-year Gate-Length cycle
 - *Possible* Intro Size Increase delays to IntER-Generation Production timing
 - *Possible* Product-Generation timing slips
 - *Possible* Radical transistor designs required? (PIDS, Design, FEP TWGs)

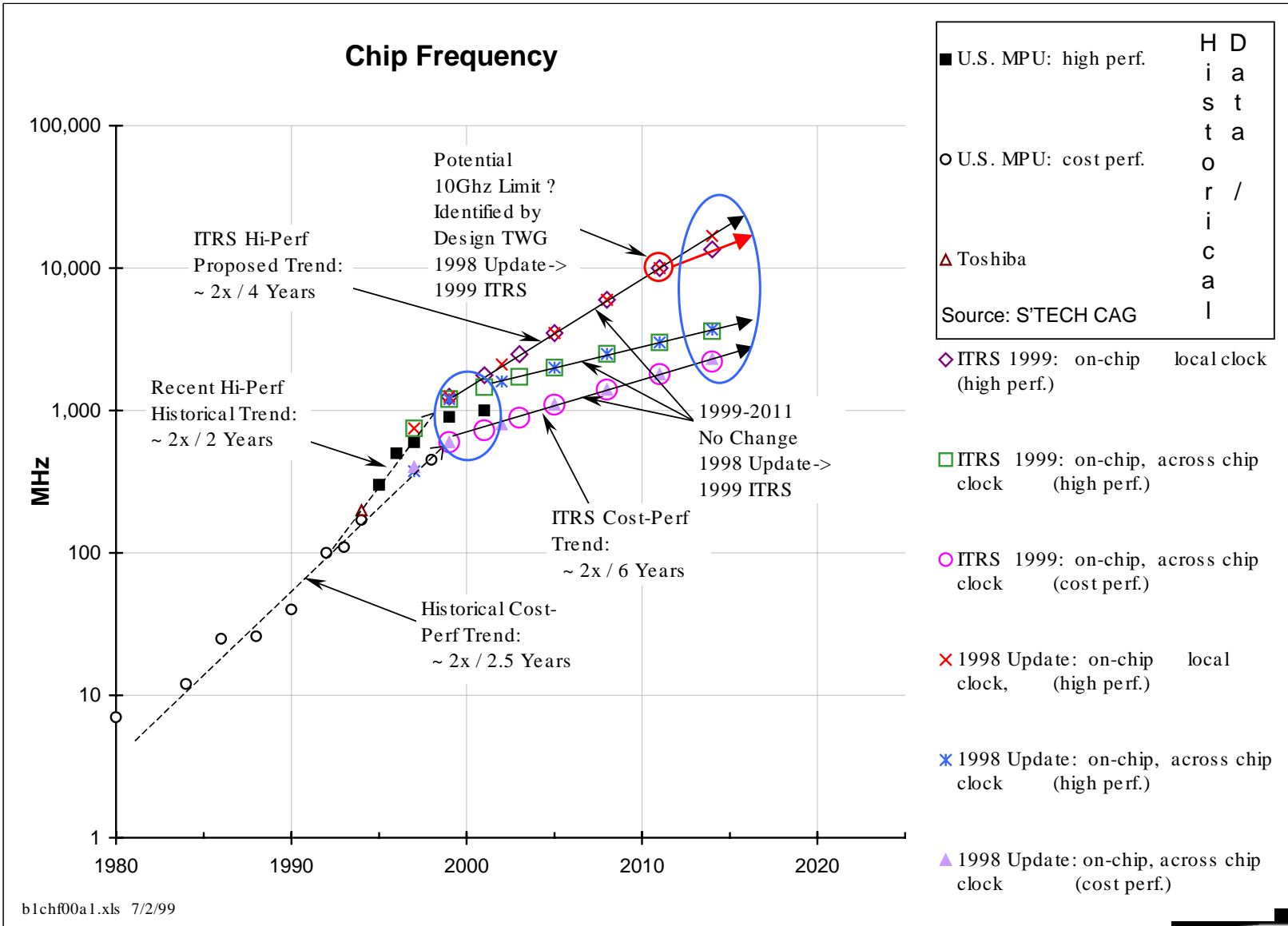
Chip Density: Logic - 1999 ITRS Proposal



Chip Density: Logic - 1999 ITRS Proposal

- MPU Chip Density
 - 1999 Same as 1998 Update
 - Trend Increase to 2x / 2years
 - Consistent with Historical Data
 - High-Performance MPU ~ 3x as Dense as Cost-Performance
- ASIC [Lo-Volume, Hi-Performance] Chip Density
 - 1999 (7/7 Update) Corrected to be Less than Hi-Performance MPU
 - Proposed Growth Trend Same as MPU - 2x / 2years
 - Faster than Previous 1998 Update Rate, but Slower than Recent History

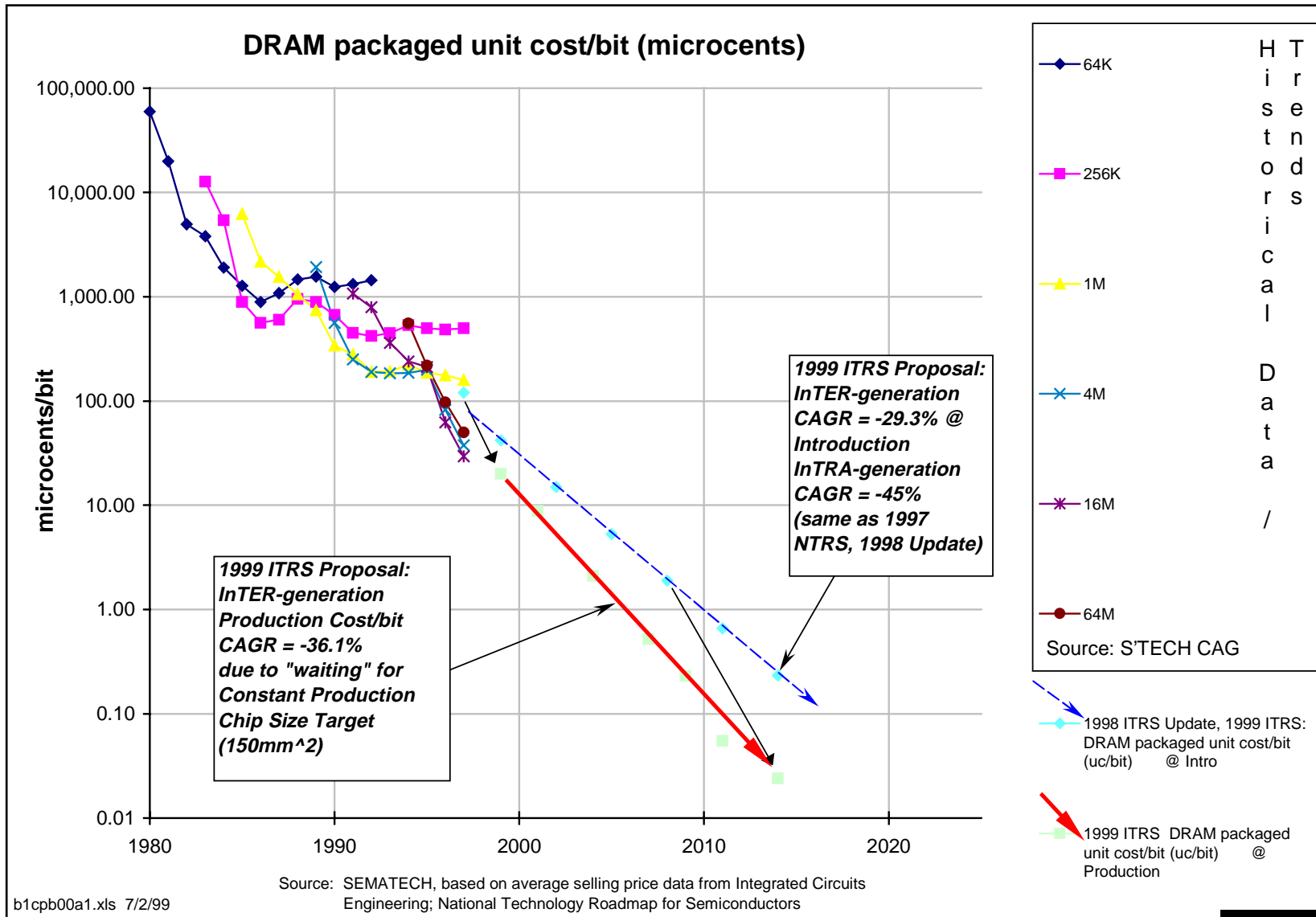
Chip Frequency: Logic - 1999 ITRS Proposal



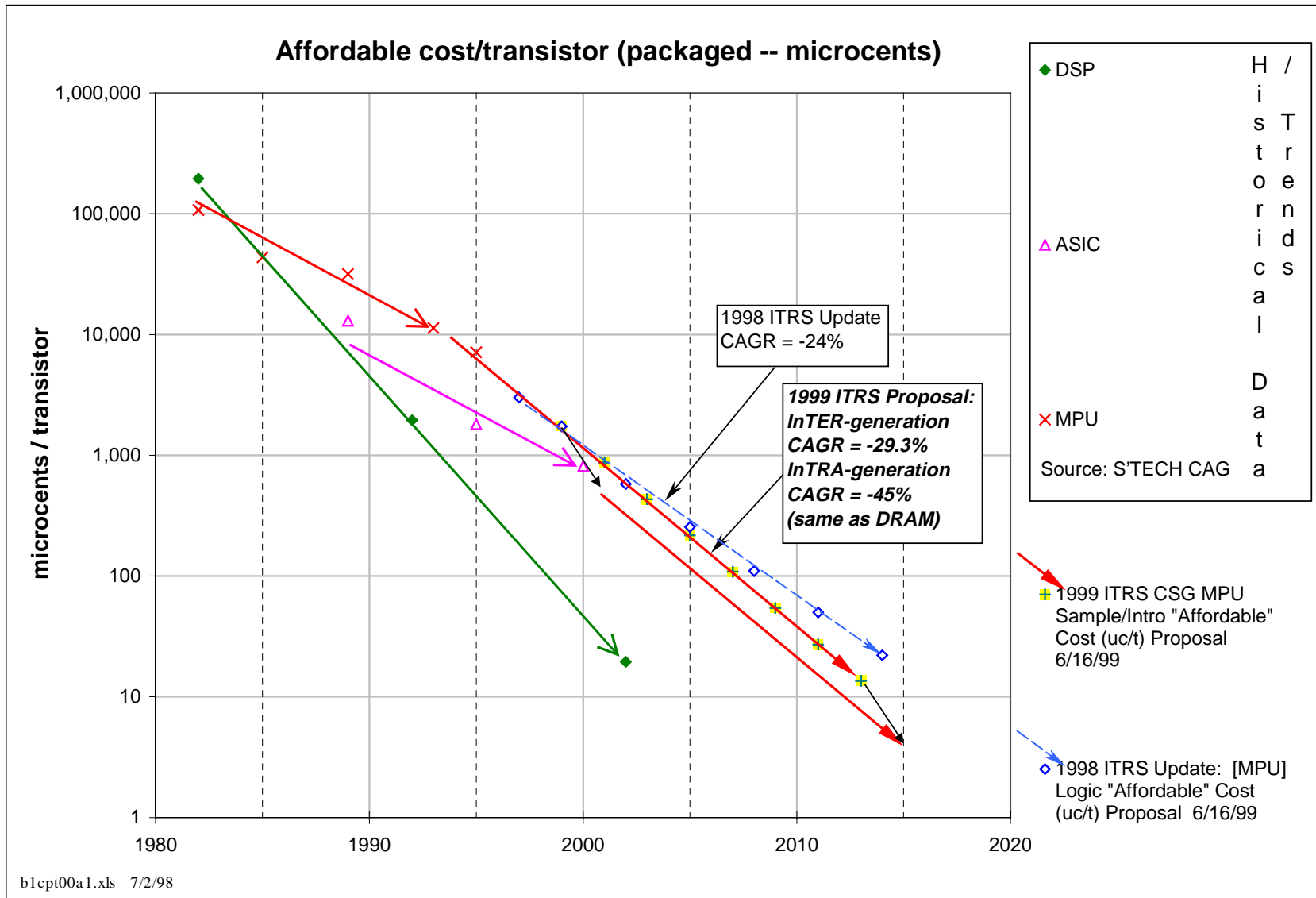
Chip Frequency: Logic - 1999 ITRS Proposal

- MPU Chip Frequency
 - 1999 ITRS Proposal from Design TWG Same as 1998 Update for 1999-2011
 - Potential Challenge Identified at 2011 to Frequencies Above 10Ghz
 - Trend for On-Chip Core High-Performance: ~ 2x / 4 years
 - Slower than Recent Historical Data ~ 2x / 2 Years
 - Cost-Performance MPU Trend ~ 2x / 6 years
 - Slower than Long History of 2x / 2.5 years
 - Trend for High-Performance Across-Chip ~ Same as Cost Performance
 - But @ ~ 2x Faster Level

“Affordable” Cost: 1999 ITRS Proposal - DRAM



“Affordable” Cost: 1999 ITRS Proposal - Logic



“Affordable” Cost: 1999 ITRS Proposal

- DRAM “Affordable” Cost/bit
 - 35% Commodity Gross Profit Margin assumed
 - InTER-Generation Intro cost/bit same as 1998 Update (-29.3% per year)
 - InTRA-Generation reduction rate same as 1998 Update (-45% per year)
 - InTER-Generation Production cost/bit trend steeper (-39.1% per year) due to “waiting” for constant die size target (150mm²) to be achieved
- MPU “Affordable” Cost/transistor
 - InTER-Generation Intro cost/bit steeper (same as DRAM: -29.3% per year)
 - Consistent with recent history
 - InTRA-Generation reduction rate same as 1998 Update (-45% per year)

ORTC Summary

- Technology Node Consensus Achieved at Munich
 - Additional 1-Year DRAM Node Pull-in at 130nm Proposed
- Chip Size Trend Consensus Achieved, but Affordable/Timely Chip Sizes at Risk
 - Cell Design Solutions required
 - Pressure to Pull-in / Accelerate will continue
- ASIC Density Accelerated - Consistent w/MPU

ORTC Summary (cont.)

- Chip Frequency Slowing - Limit @ 10Ghz?
- “Affordability” Pressure Increasing
 - MPU on DRAM (-29.3%) Rate,
 - DRAM Production-Level Decrease Rate Requires Update to new Chip Size Proposal
- Plans
 - Final ORTC/ITWG Table Integration
 - Draft Reviews/Approval
 - Publication