

- 
- 
- 
- 
- 
- 
- 

# Interconnect Working Group



Christopher Case  
8 July 1999  
Santa Clara, CA



- 
- 
- 
- 
- 
- 
- 
- 

International Technology Roadmap for Semiconductors





**1998/9**

**Membership**

**Christopher Case, chair    Bob Havemann, co-chair**

**Marilyn Jones  
SEMATECH**



**Bob Geffken, ITWG co-chair**

**Applied Materials  
Sam Broydo**

**Stanford  
Simon Wong**

**Gary Ray**

**SRC  
Jim Hutchby**

**Steve Burke**

**Dennis Hartman**

**Conexant  
Maureen Brongo**

**U of New Mexico  
Joe Cecchi**

**Nat'l Institute of Standards  
Harry Schafft**

**International Technology Roadmap for Semiconductors**



# ITWG Participation

Name/Region	Affiliation	Telephone	Telefax	E-Mail
<i>Europe</i>				
<b>Gerhard Göltz</b>	STMicroelectronics	33-47-692-6094		gerhard.goltz@st.com
<b>Hans Barth</b>	Infineon			
<i>Japan</i>				
<b>Riichirou Aoki</b>	Selete	81-45-866-6817	81-45-866-6880	aoki@cm.selete.co.jp
<b>Shinichi Ogawa</b>	Matsushita Electronics	81-75-662-8455	81-75-662-6154	shinichi_ogawa@roy.hi-ho.ne.jp
<i>Korea</i>				
	Reps at Munich and Santa Clara			
<i>Taiwan</i>				
<b>Calvin Hsueh</b>	Macronix	886-3-5786688	886-3-5632888	calvinhsued@mxic.com.tw
<b>Shin-Puu Jeng</b>	WSMC	886-3-5678888	886-3-5662059	sp.jeng@wsmc.com.tw
<i>US</i>				
<b>Robert Geffken</b>	IBM	802 769 8613	802-769-9659	rgeffken@us.ibm.com
<b>Christopher Case</b>	Lucent - Bell Labs	908 582 2941	908 582 2300	christopher.j.case@bell-labs.com

# Key Team Contacts

Section	Affiliation	Telephone	Tele fax	E-Mail
<i>Overview</i>				
Christopher Case	Lucent	908/582 2941	908/582 2300	christopher.j.case@bell-labs.com
Robert Have mann	SEMATECH/TI	512/356-7824	512/356-3219	bob.have mann@se mate ch.org
<i>Dielectrics</i>				
Steve Burke	Intel	408/765-2161	408/765-2554	steven.robert.burke@intel.com
Maurenn Brongo	Conexant	949/483-4958	949/483-6104	maureen.brongo@conexant.com
<i>Conductors</i>				
Robert Geffken	IBM	802/769 8613	802/769-9659	rgeffken@us.ibm.com
Christopher Case	Lucent	908/582 2941	908/582-2300	christopher.j.case@bell-labs.com
<i>Planarization</i>				
Gary Ray	HP	650/857-5475	650/857-6684	gary_ray@hpl.hp.com
Maurenn Brongo	Conexant	949/483-4958	949/483-6104	maureen.brongo@conexant.com
<i>Etch</i>				
Dennis Hartman	Motorola	512/933-5167	512/933-5497	rrwa80@email.sps.mot.com
Joe Cecci	Univ.N.Mexico	505/277-5431	505/277-5433	cecchi@unm.edu
<i>Reliability</i>				
Robert Have mann	SEMATECH/TI	512/356-7824	512/356-3219	bob.have mann@se mate ch.org
Harry Schafft	NIST	650/725-3706	650/725-3383	harry.schafft@nist.gov
<i>Sys. &amp; Perf. Issues</i>				
Jim Hutchby	SRC	919/941-9450	919/941-9451	hutchby@src.org
Simon Wong	Stanford	650/724-3383	650/725-3706	wong@ee.stanford.edu
Robert Have mann	SEMATECH/TI	512/356-7824	512/356-3437	bob.have mann@se mate ch.org

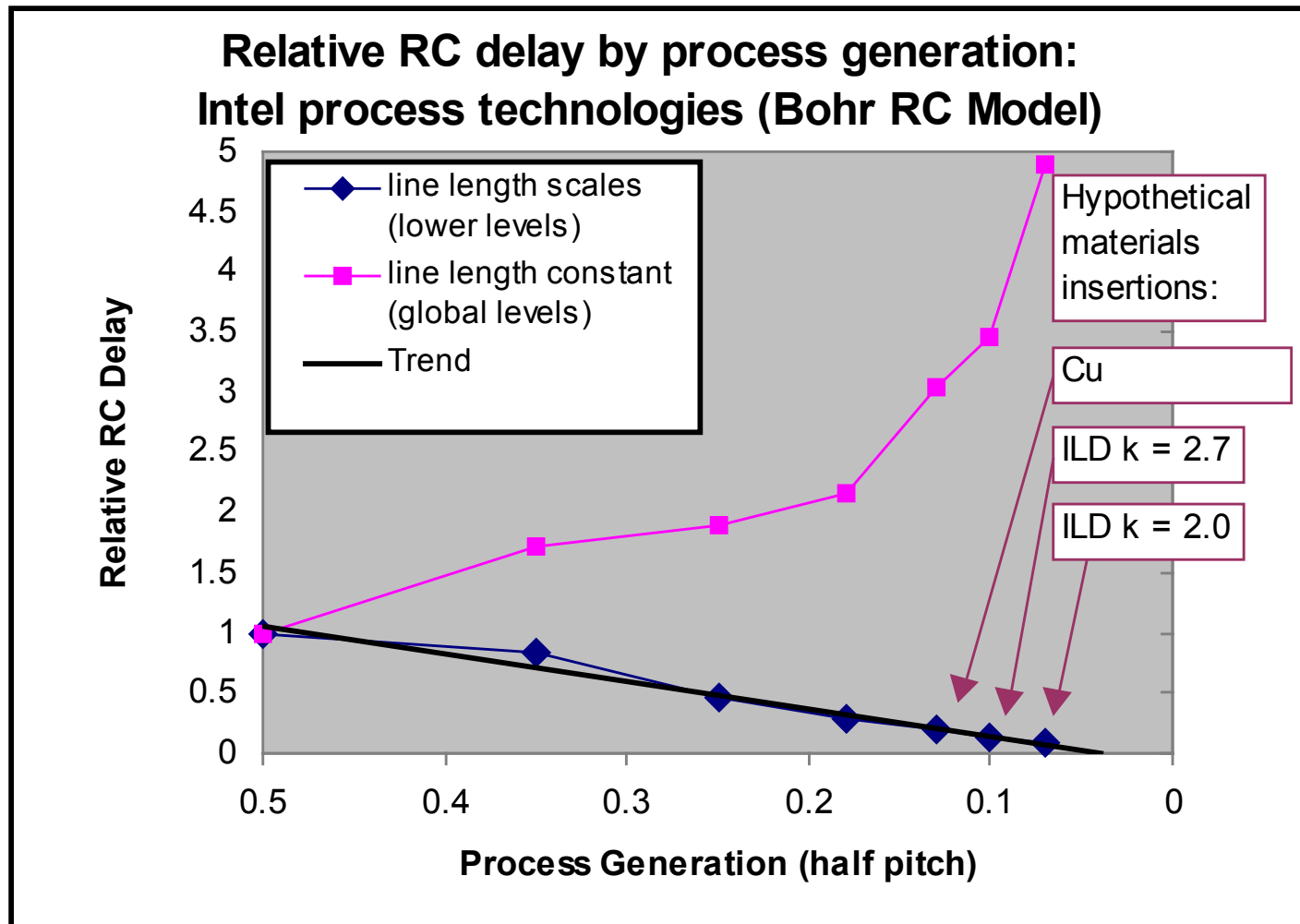
International Technology Roadmap for Semiconductors



# Interconnect Progression

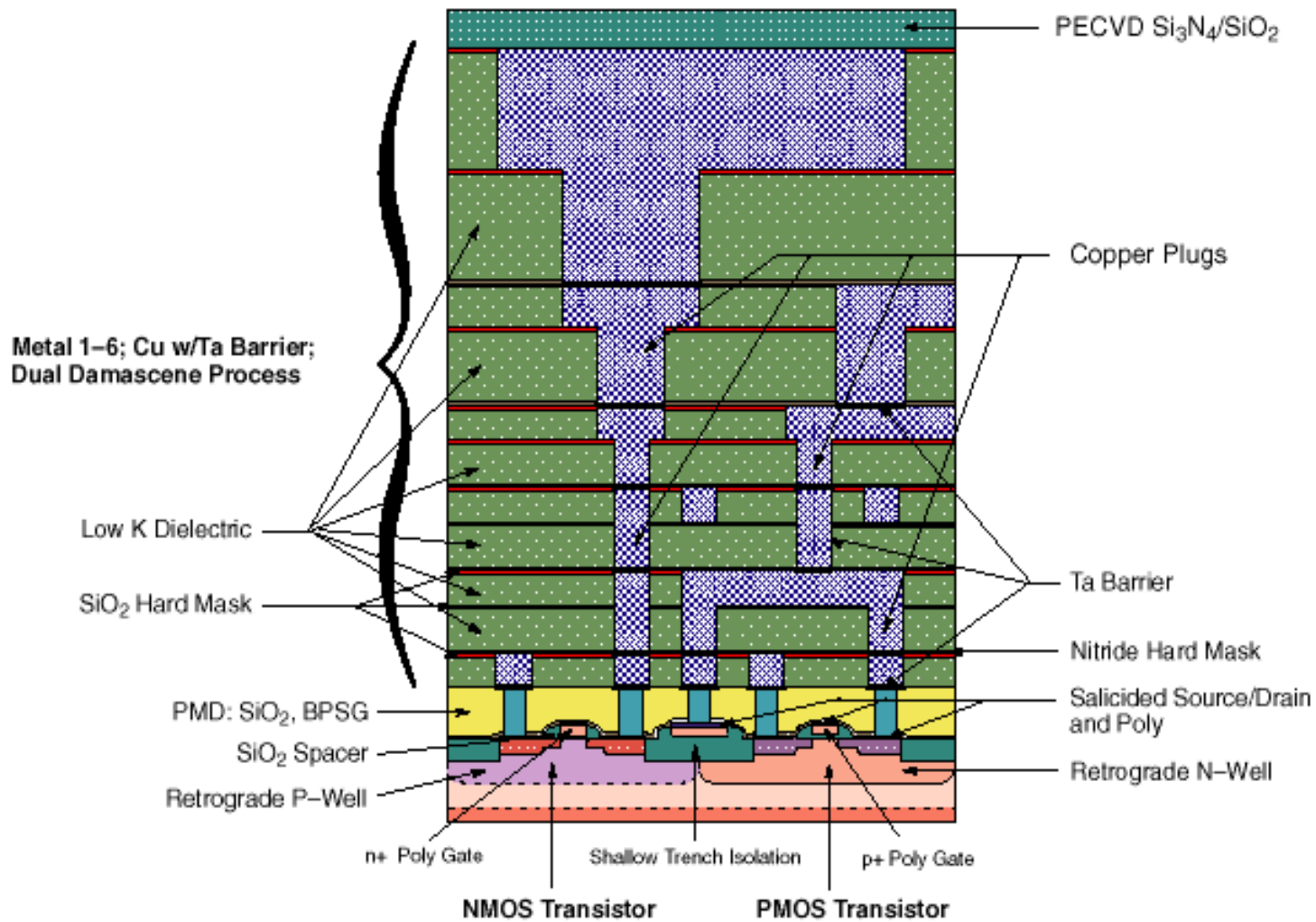
- 1994 NTRS introduced the need for Cu and low  $\kappa$  materials
- 1997 NTRS describes the adoption of these materials
- 1999 ITRS highlighted
  - Rapid changes in materials
  - Materials solutions alone cannot deliver performance - end of traditional scaling in sight

# No Moore Scaling!



Legend
x is to scale
y is 10x above Si; real AR's = 3-4:1

### 0.18 $\mu\text{m}$ Device Cross Section – High Performance Logic



International Technology Roadmap for Semiconductors



# Difficult Challenges

## >100 nm

- New materials
- Reliability
- Process integration
- Dimensional control
- Interconnect process with low/no device impact

## <100 nm

- Dimensional control
- Aspect ratios for fill and etch
- New materials and size effects
- Process integration
- Solutions beyond copper and low  $\kappa$

# Materials Challenges

- Short term
  - Rapid introduction of materials
    - new barriers and seed layers
      - in situ formed dielectric and metal
    - new dielectrics (both low and high k)
    - ferroelectrics
  - Combination of materials and technologies
    - to address SOC needs
  - Many new reliability challenges
    - new materials and interfaces
    - electrical, thermal and mechanical exposure

# Materials Challenges

- Long term
  - Continued introduction of materials
    - barriers seed layers for optical, low temp, rf, air gap
    - conducting polymers, cooled conductors, alternate metals, superconductors
  - More reliability challenges
  - Microstructural and atom scale effects

# Dimensional Control

- Multi-dimensional control of features
  - performance and reliability implications
- Multiple levels
  - reduced feature size, new materials and pattern dependent processes
  - process interactions
    - CMP and deposition - dishing and erosion
    - Deposition and etch - to pattern multi-layer dielectrics
- Aspect ratios for etch and fill
  - particularly DRAM contacts and dual damascene

# Process Integration

- Combinations and interactions of new materials and technologies
  - interfaces, contamination, adhesion, diffusion, leakage concerns, thermal budget, ESH, CoO
- Structural complexity
  - levels - interconnect, ground planes, decoupling capacitors
  - passive elements
  - other SOC interconnect design needs (rf)
  - cycle time

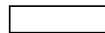
# Solutions beyond Cu and low $\kappa$

- Material innovation combined with traditional scaling will no longer satisfy performance requirements
  - Design, packaging and interconnect innovation needed
  - What's next?
    - optical, rf, low temperature
    - novel active devices (3D or multi-level)

# MPU Short Term Requirements

<i>YEAR OF INTRODUCTION</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>
MPU pitch	230	210	180	160	145	130	115
MPU gate length (nm)	140	120	100	85	80	70	65
Number of metal levels	6-7	7	7-8	7-8	7-8	8	8
Number of optional levels – ground planes/capacitors	2	2	2	2	2	2	2
Local wiring pitch (nm)	500	450	405	365	330	295	265
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2		
Local wiring A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.7
Cu local dishing (nm), 5% x height	18	16	15	14	13	12	11

*Solutions Exist*



*Solutions Being Pursued*



*No Known Solutions*



International Technology Roadmap for Semiconductors



# MPU Short Term Requirements (contd)

<i>YEAR OF INTRODUCTION</i> <i>"TECHNOLOGY NODE"</i>	<i>1999</i> <i>180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002</i> <i>130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005</i> <i>100 nm</i>
Intermediate wiring pitch (nm)	640	575	520	465	420	375	340
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6		
Intermediate wiring dual damascene A/R (Cu)	4.1	4.2	4.3	4.3	4.4	4.5	4.6
Cu intermediate dishing (nm), 15 micron line, 20% x height	102	98	94	84	80	75	71
Dielectric erosion, intermediate, 50% density, 15% x height	77	74	71	63	60	56	53
Minimum global wiring pitch (nm)	1050	945	850	765	690	620	560
Global wiring A/R (Al)	2	2.1	2.2	2.3	2.4		
Global wiring A/R (Cu)	1.5	1.6	1.7	1.7	1.8	1.9	2
Cu global dishing (nm), 15 micron line, 20% x height	158	151	145	130	124	117	112
Minimum metal effective resistivity - cm) Al wiring*	3.3	3.3	3.3	3.3	3.3		
Minimum metal effective resistivity ( $\mu\Omega$ -cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (conformal) (nm)	23	19	16	13	11	7	3
Interlevel metal insulator - effective dielectric constant ( $\kappa$ )	3.5 - 4.0	3.5 - 4.0	2.7 - 3.5	2.7 - 3.5	2.2 - 2.7	2.2 - 2.7	1.6 - 2.2

*Solutions Exist*

*Solutions Being Pursued*

*No Known*

International Technology Roadmap for Semiconductors




# MPU Long Term Requirements

<i>YEAR OF INTRODUCTION "TECHNOLOGY NODE"</i>	<i>2008 70 nm</i>	<i>2011 50 nm</i>	<i>2014 35 nm</i>
MPU pitch	<b>80</b>	<b>55</b>	<b>40</b>
MPU gate length (nm)	<b>45</b>	<b>32</b>	<b>22</b>
Number of metal levels	<b>9</b>	<b>10</b>	<b>11</b>
Number of optional levels – ground planes/capacitors	<b>2</b>	<b>2</b>	<b>2</b>
Jmax (A/cm <sup>2</sup> ) - wire	<b>2.4E6</b>	<b>4.0E6</b>	<b>6.6E6</b>
Jmax (mA) - via	<b>0.24</b>	<b>0.20</b>	<b>0.17</b>
Local wiring pitch (nm)	<b>185</b>	<b>130</b>	<b>95</b>
Local A/R (for Cu)	<b>1.9</b>	<b>2.1</b>	<b>2.3</b>
Cu local dishing (nm), 5% x height	<b>9</b>	<b>7</b>	<b>5</b>

*Solutions Exist* 

*Solutions Being Pursued* 

*No Known Solutions* 

# MPU Long Term Requirements (contd)

<i>YEAR OF INTRODUCTION "TECHNOLOGY NODE"</i>	<i>2008 70 nm</i>	<i>2011 50 nm</i>	<i>2014 35 nm</i>
Intermediate wiring pitch (nm)	240	165	115
Intermediate wiring dual damascene A/R (Cu)	4.8	5.1	5.4
Cu intermediate dishing (nm), 15 micron line, 20% x height	55	43	33
Dielectric erosion, intermediate, 50% density, 15% x height	0	0	0
Minimum global wiring pitch (nm)	390	275	190
Global wiring A/R (Cu)	2.4	2.7	3.0
Cu global dishing (nm), 15 micron line, 20% x height	94	74	57
Minimum metal effective resistivity ( $\Omega$ -cm) Cu wiring*	1.8	=1.8	=1.8
Barrier/cladding thickness (conformal) (nm)	0	0	0
Interlevel metal insulator - effective dielectric constant (k)	1.5	=1.5	=1.5

Effective  $\kappa$  less than 1.5 have **No Known Solutions**

*Solutions Exist*



*Solutions Being Pursued*



*No Known Solutions*




International Technology Roadmap for Semiconductors




# SOC Short Term Requirements

<i>YEAR OF INTRODUCTION</i> <i>"TECHNOLOGY NODE"</i>	<i>1999</i> <i>180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002</i> <i>130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005</i> <i>100 nm</i>
MPU pitch (nm)	230	210	180	160	145	130	115
ASIC gate (nm)	180	165	150	130	120	110	100
Number of metal levels	6	6	7	7	7-8	8	8
Number of optional levels – passive elements	0	0	2	2	4	4	4
Local wiring pitch (nm)	450	405	360	325	290	260	230
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2		
Local wiring A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.7
Intermediate wiring pitch (nm)	560	505	450	405	360	325	285

*Solutions Exist* 

*Solutions Being Pursued* 

*No Known Solutions* 

SOC characterized by more aggressive local pitch than MPU

Passive elements require the use of more levels of metal


International Technology Roadmap for Semiconductors




# SOC Short Term Requirements

<i>YEAR OF INTRODUCTION</i> <i>"TECHNOLOGY NODE"</i>	<i>1999</i> <i>180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002</i> <i>130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005</i> <i>100 nm</i>
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6		
Intermediate via A/R (Al)	2.8	2.8	2.9	2.9	3.0		
Intermediate wiring dual damascene A/R (Cu)	4.1	4.2	4.3	4.3	4.4	4.5	4.6
Global wiring pitch (nm)	900	810	720	650	580	520	460
Global wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6		
Global wiring A/R (Cu)	1.6	1.6	1.7	1.7	1.8		
Global wiring dual damascene A/R (Cu)	3.8	3.9	4.0	4.0	4.1	4.2	4.3
Interlevel metal insulator - effective dielectric constant ( $\kappa$ )	3.5 - 4.0	3.5 - 4.0	2.7 - 3.5	2.7 - 3.5	2.2 - 2.7	2.2 - 2.7	1.6 - 2.2

*Solutions Exist* 

*Solutions Being Pursued* 

*No Known Solutions* 

International Technology Roadmap for Semiconductors



# SOC Long Term Requirements

<i>YEAR OF INTRODUCTION "TECHNOLOGY NODE"</i>	<i>2008 70 nm</i>	<i>2011 50 nm</i>	<i>2014 35 nm</i>
MPU pitch (nm)	<b>80</b>	<b>55</b>	<b>40</b>
ASIC gate (nm)	<b>70</b>	<b>50</b>	<b>35</b>
Number of metal levels	<b>9</b>	<b>10</b>	<b>11</b>
Number of optional levels – passive elements	<b>6</b>	<b>6</b>	<b>6</b>
Local wiring pitch (nm)	<b>165</b>	<b>120</b>	<b>85</b>
Local wiring A/R (for Cu)	<b>1.9</b>	<b>2.1</b>	<b>2.2</b>
Intermediate wiring pitch (nm)	<b>210</b>	<b>145</b>	<b>110</b>
Intermediate wiring dual damascene A/R (Cu)	<b>4.8</b>	<b>5.1</b>	<b>5.4</b>
Global wiring pitch (nm)	<b>330</b>	<b>240</b>	<b>170</b>
Global wiring dual damascene A/R (Cu)	<b>4.5</b>	<b>4.9</b>	<b>5.2</b>
Interlevel metal insulator - effective dielectric constant ( $\kappa$ )	<b>1.5</b>	<b>1.5</b>	<b>1.5</b>

*Solutions Exist*

*Solutions Being Pursued*

*No Known Solutions*

International Technology Roadmap for Semiconductors



# DRAM Short Term Requirements

Up to 4 interconnect levels

<i>YEAR OF INTRODUCTION</i> <i>"TECHNOLOGY NODE"</i>	<i>1999</i> <i>180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002</i> <i>130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005</i> <i>100 nm</i>
DRAM pitch	<b>180</b>	<b>165</b>	<b>150</b>	<b>130</b>	<b>120</b>	<b>110</b>	<b>100</b>
Number of metal levels	<b>3</b>	<b>3</b>	<b>3</b>	<b>3-4</b>	<b>4</b>	<b>4</b>	<b>4</b>
Contact A/R – stacked capacitor	<b>6.3</b>	<b>6.7</b>	<b>7.1</b>	<b>7.5</b>	<b>8.0</b>	<b>8.5</b>	<b>9.0</b>
Local wiring pitch (nm) non-contacted	<b>360</b>	<b>330</b>	<b>300</b>	<b>260</b>	<b>240</b>	<b>210</b>	<b>200</b>
Specific contact resistance ( $\Omega\text{-cm}^2$ )	<b>6E-7</b>			<b>3E-7</b>			<b>2E-7</b>
Specific via resistance ( $\Omega\text{-cm}^2$ )	<b>7E-9</b>			<b>2E-9</b>			<b>1E-9</b>
Metal effective resistivity ( $\mu\Omega\text{-cm}$ )	<b>3.3</b>	<b>3.3</b>	<b>3.3</b>	<b>3.3</b>	<b>3.3</b>	<b>3.3</b>	<b>2.2</b>
Interlevel metal insulator - effective dielectric constant ( $\kappa$ )	<b>4.1</b>	<b>4.1</b>	<b>4.1</b>	<b>3.0 - 4.1</b>	<b>3.0 - 4.1</b>	<b>3.0 - 4.1</b>	<b>2.5 - 3.0</b>

*Solutions Exist*

*Solutions Being Pursued*

*No Known Solutions*

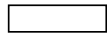
International Technology Roadmap for Semiconductors



# DRAM Long Term Requirements

<i>YEAR OF INTRODUCTION "TECHNOLOGY NODE"</i>	<i>2008 70 nm</i>	<i>2011 50 nm</i>	<i>2014 35 nm</i>
DRAM pitch	<b>70</b>	<b>50</b>	<b>35</b>
Number of metal levels	<b>4</b>	<b>4</b>	<b>4</b>
Contact A/R – stacked capacitor	<b>10.5</b>	<b>12</b>	<b>13.5</b>
Local wiring pitch (nm) non-contacted	<b>140</b>	<b>100</b>	<b>70</b>
Specific contact resistance ( $\Omega\text{-cm}^2$ )	<b>8E-8</b>	<b>3E-8</b>	<b>2E-8</b>
Specific via resistance ( $\Omega\text{-cm}^2$ )	<b>6E-10</b>	<b>3E-10</b>	<b>1.5E-10</b>
Metal effective resistivity ( $\mu\Omega\text{-cm}$ )	<b>2.2</b>	<b>2.2</b>	<b>2.2</b>
Interlevel metal insulator - effective dielectric constant (k)	<b>2.5 - 3.0</b>	<b>2.0 - 2.5</b>	<b>2.0 - 2.3</b>

*Solutions Exist*



*Solutions Being Pursued*



*No Known Solutions*



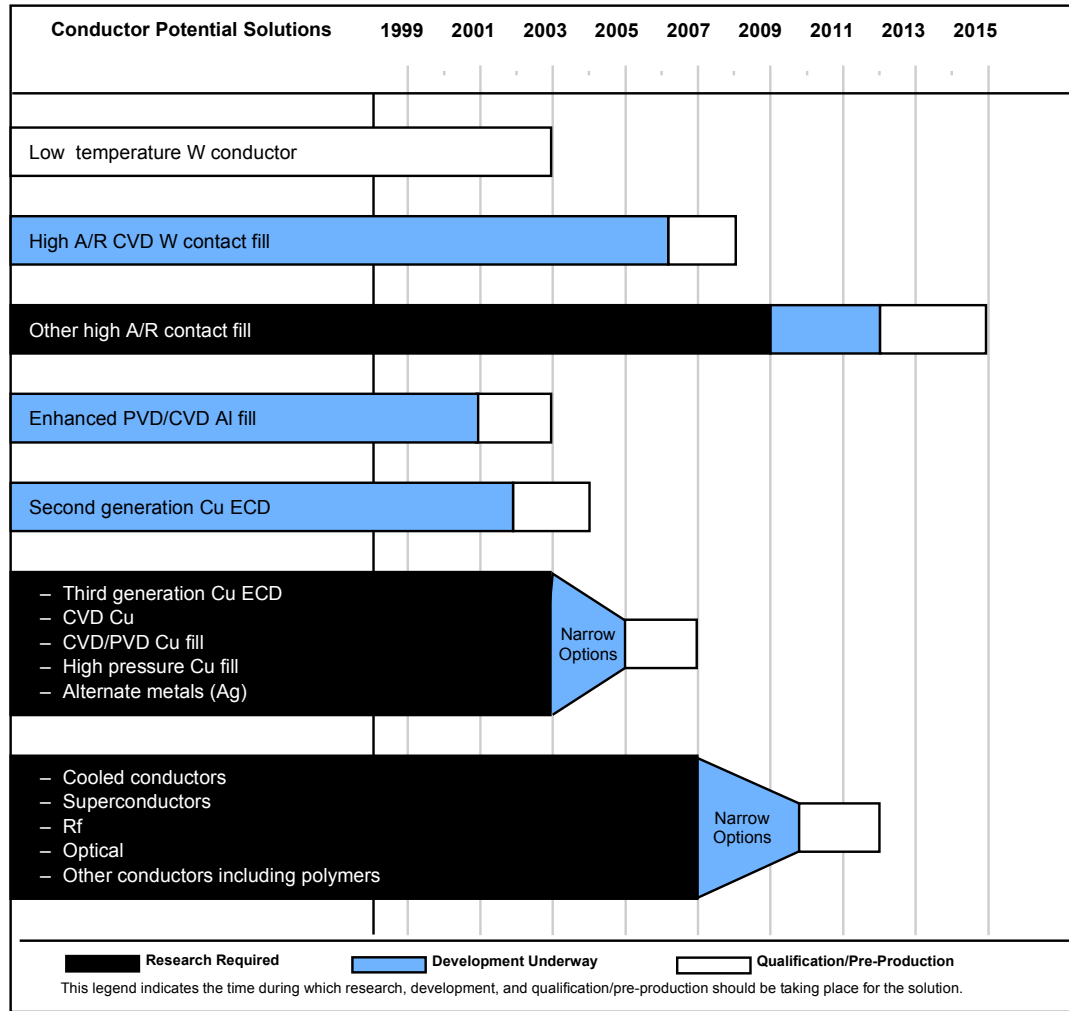
**No Known Solutions to A/R**

**High k materials may provide some relief**

International Technology Roadmap for Semiconductors



# Conductor Potential Solutions



## Challenges

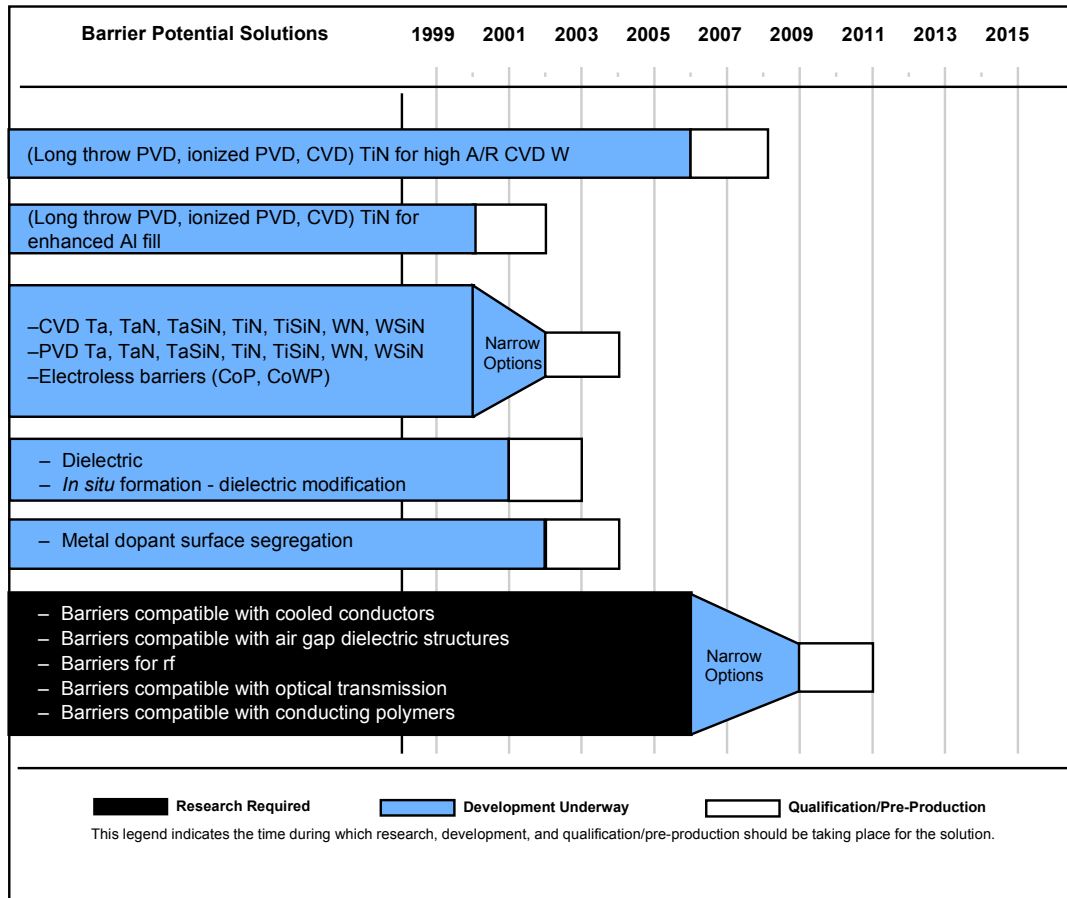
Low temp CVD W for low  $\kappa$  compatibility

High A/R contact fill for DRAM

Cu fill of dual damascene structures with reduced CD and high A/R

Identifying and implementing solutions after Cu and low  $\kappa$

# Barrier Potential Solutions



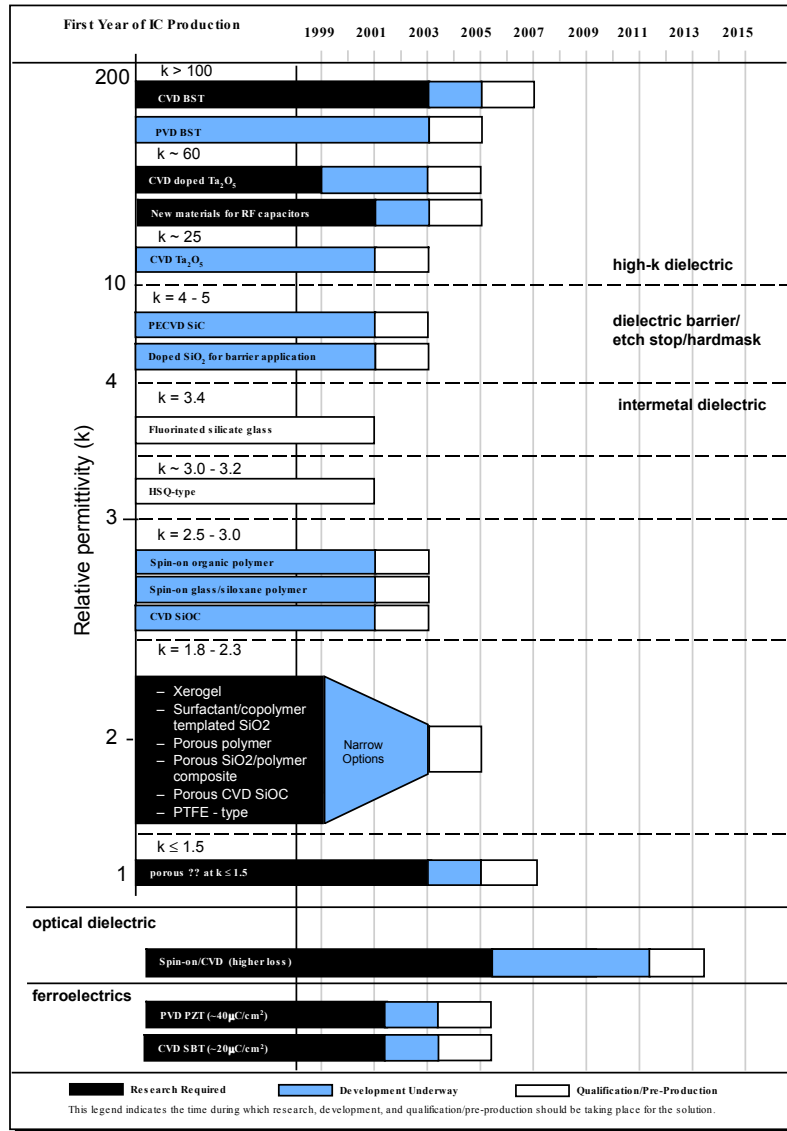
## Challenges

**Solutions for high A/R  
DRAM contacts**

**Conformal barriers for  
dual damascene Cu - thin,  
effective diffusion barrier,  
low via resistance**

**Barrier free solutions to  
reduce effective Cu  
resistivity**

# Dielectric Potential Solutions



## Challenges

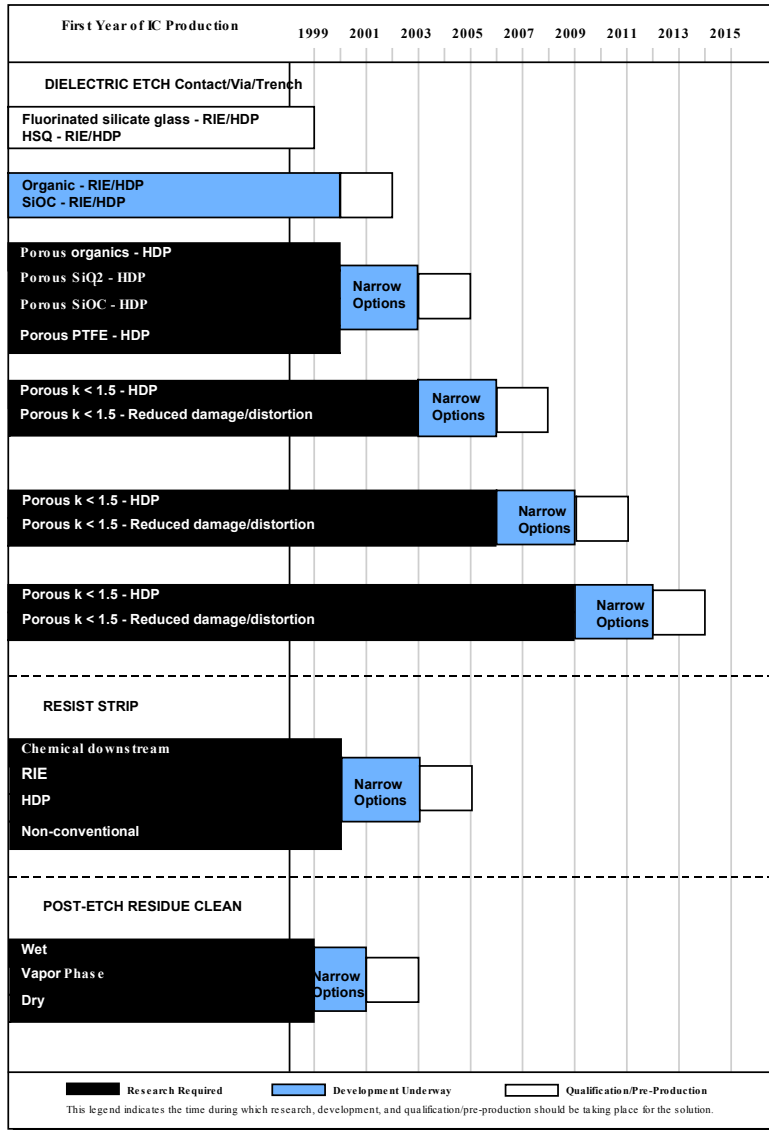
High  $\kappa$  and ferroelectrics materials development

Development and integration of ultra low  $\kappa$  materials with acceptable mechanical/thermal properties

Fabricating low-temp low-loss SiO<sub>2</sub> optical interconnect

Addressing turning radius of lossy polymer optics

# Etch Potential Solutions



## Challenges

**Dimensional control with small features and high A/R**

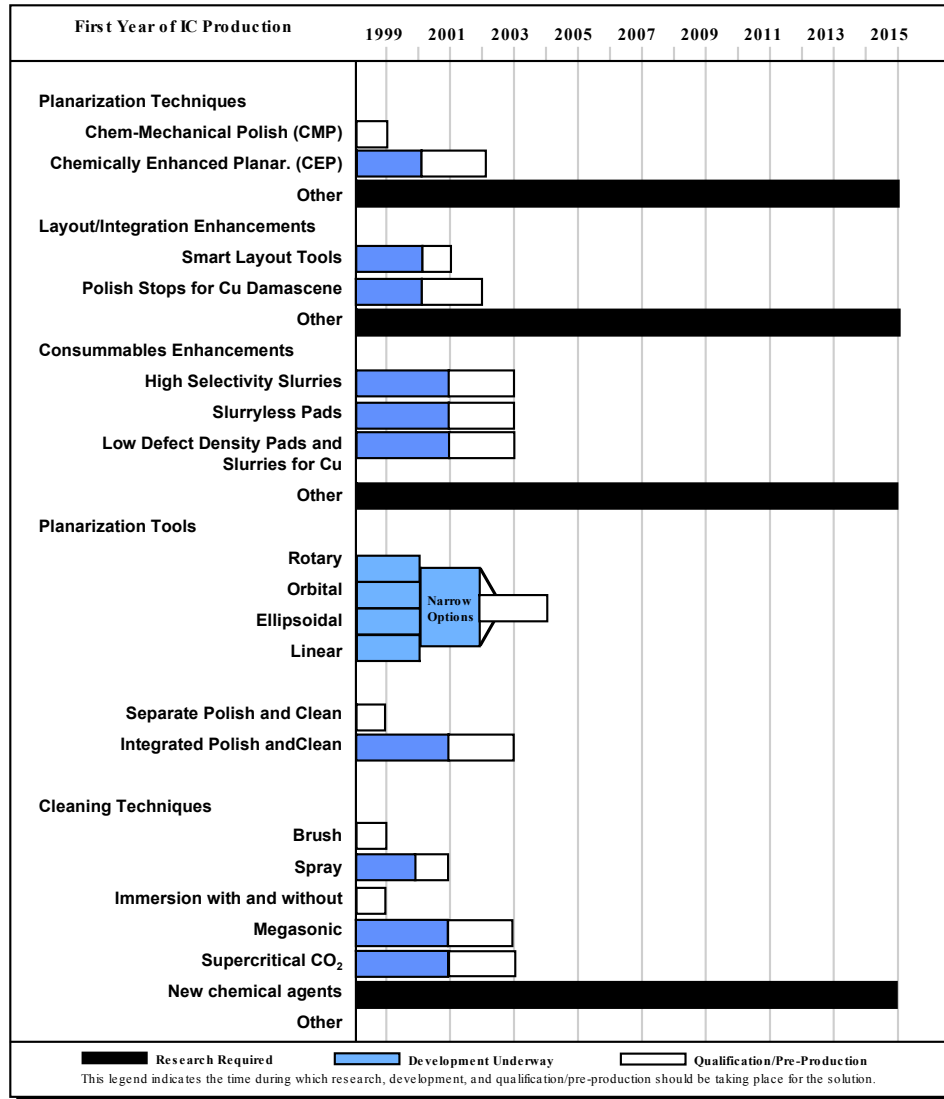
**Selectivity to etch stops and hard masks**

**Many new low and high  $\kappa$  materials - may require new chemistries**

**Strip/clean compatibility with these new materials**

**Low damage**

# Planarization Potential Solutions



## Challenges

Continued development of tools/slurries/pads

Cleaning technologies

Many new low and high  $\kappa$  materials - may require new planarization approaches

Pattern dependent planarization

Planarization over passive elements for SOC

# Long term prospective

- Cu/low k interconnects extendable for local/intermediate wiring
  - Crosstalk must be carefully managed
  - Dimensional effects at  $< 50$  nm
- Alternatives needed for global wiring
  - Design solutions (repeaters, new architectures...)
  - Coplanar waveguides or free space rf
  - Optical interconnects

# Complexity

- Complexity of connectivity a looming issue
  - Exceeding CAD tool capability & package pinout
  - SOC may alleviate
- 3D structures (active and interconnect) may alleviate the connectivity dilemma

# Coplanar Waveguides

- Key advantages include:
  - High bandwidth
  - Low frequency dispersion and low loss
  - Modular interconnect compatibility/connectivity
  - Compatibility with traditional on-chip and off-chip interconnect technologies
- Key disadvantages include:
  - Signal coupling/matching
  - Circuit complexity (noise figure)

# Free space rf interconnects

- Key advantages include
  - High bandwidth
  - Low frequency dispersion and low loss
  - Modular interconnect including compatibility with traditional on-chip and off-chip interconnect technologies
- Key disadvantages include
  - Signal discrimination
  - Circuit complexity

# Optical Interconnects

- Key advantages include:
  - High bandwidth
  - No frequency-dependent loss or crosstalk
  - No distance-dependent loss or degradation
  - Modular interconnect compatibility/connectivity
  - Compatibility with off-chip optical communications
- Key disadvantages include:
  - Process complexity/cost
  - Additional power needed (especially for receiver circuit)

# Last words

- Rapid changes in materials
- Materials solutions alone cannot deliver performance - end of traditional scaling
- System level solutions must be accelerated
- System on a Chip implementations will propagate
- Optical/rf/waveguide/3D current alternatives