Process Integration, Devices & Structures (PID&S)

Working Group Report Summary

April 13, 1999

Contributors to the PID&S TWG Process

• Bob Eklund	TI
• Nobuhiro Endo	NEC
• Carel van der Poel	Philips
• Steve Hillenius	Lucent
• Gerrit Lange	Infineon
• Jack Sun	TSMC
• Jae Chul Om	Hyundai

Three Issues to Highlight

SOC Issues:

Performance Limits on Transistors
Embedded Combinations critical for development
Predicting choices drive development more than scaling

Chip Size Restrictions:

Power constraints limit chip size for logic
Maximum Chip size may remain constant

Gate Dielectric Dilemma:

SiO_2 Scaling faster (1 node)
Alternative dielectric/electrodes late (~5 yrs)

Chip Size Limited by Power Constraints:

	TWG Technology Requirements						
	TBD *180 nm*	*TBD* *130 nm*	*TBD* *100 nm*	*TBD* *70 nm*	*TBD* *50 nm*	*TBD* *35 nm*	*TBD* *25 nm*
Min. Logic V_{dd} (V) (desktop)	**1.5 - 1.8**	**1.2 - 1.5**	**0.9 - 1.2**	**0.6 - 0.9**	**0.5 - 0.6**	**0.3 - 0.6**	**0.3 - 0.6**
Tox equivalent (nm)	**1.9–2.5**	**1.5-1.9**	**1.2-1.5**	**0.8-1.1**	**0.6-0.8**	**0.5-0.6**	**< 0.5**
Nominal I_{on} @ 25 °C (µA/µm) [NMOS/PMOS] High Perf.	**600/280**	**600/280**	**600/280**	**600/280**	**600/280**	**600/280**	**600/280**
Max I_{off} @ 25 °C (nA/µm) (For min. L device) High Perf.	**5**	**3**	**3**	**2**	**1**	**0.50**	**0.20**
Nominal I_{on} @ 25 °C (µA/µm) [NMOS/PMOS] Low Power	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**
Max I_{off} @ 25 °C (pA/µm) (For min. L device) Low Power	**1**	**0.4**	**0.3**	**0.2**	**0.1**	**0.05**	**0.02**

Three Issues to Highlight

SOC Issues:

Performance Limits on Transistors
Embedded Combinations critical for development
Predicting choices drive development more than scaling

Chip Size Restrictions:

Power constraints limit chip size for logic
Maximun Chip size may remain constant

Gate Dielectric Dilemma:

SiO_2 Scaling faster (1 node)
Alternative dielectrics/electrodes late (~5 yrs)

70-100nm Node may be break point:

Alternative oxide/gate late ~5yrs

	TWG Technology Requirements						
	TBD *180 nm*	*TBD* *130 nm*	*TBD* *100 nm*	*TBD* *70 nm*	*TBD* *50 nm*	*TBD* *35 nm*	*TBD* *25 nm*
Min. Logic V_{dd} (V) (desktop)	**1.5 - 1.8**	**1.2 - 1.5**	**0.9 - 1.2**	**0.6 - 0.9**	**0.5 - 0.6**	**0.3 - 0.6**	**0.3 - 0.6**
Tox equivalent (nm)	**1.9–2.5**	**1.5-1.9**	**1.2-1.5**	**0.8-1.1**	**0.6-0.8**	**0.5-0.6**	**< 0.5**
Nominal I_{on} @ 25 °C (µA/µm) [NMOS/PMOS] High Perf.	**600/280**	**600/280**	**600/280**	**600/280**	**600/280**	**600/280**	**600/280**
Max I_{off} @ 25 °C (nA/µm) (For min. L device) High Perf.	**5**	**3**	**3**	**2**	**1**	**0.50**	**0.20**
Nominal I_{on} @ 25 °C (µA/µm) [NMOS/PMOS] Low Power	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**
Max I_{off} @ 25 °C (pA/µm) (For min. L device) Low Power	**1**	**0.4**	**0.3**	**0.2**	**0.1**	**0.05**	**0.02**

Three Issues to Highlight

SOC Issues:

Performance Limits on Transistors
Embedded Combinations critical for development
Predicting choices drive development more than scalir

Chip Size Restrictions:

Power constraints limit chip size for logic
Maximum Chip size may remain constant

Gate Dielectric Dilemma:

SiO_2 Scaling faster (1 node)
Alternative dielectrics/electrodes late (~5 yrs)
Roadmap may be delayed until Dielectric available