

Overall Roadmap Technology Characteristics Tables
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Notations relevant to each sheet:

Below, based on the outcome of the 12/10,11 ITWG/IRC Meetings, is my understanding of what the 1998 ITRS Update [1999(a) ITRS Kickoff] header tables should look like (DRAM Half-pitch-based Nodes, 3-Year Cycle):

Node Header		ITRS NODE	ITRS NODE	ITRS NODE	ITRS NODE	ITRS NODE	ITRS NODE
	ITEM	1999	2002	2005	2008	2011	2014
	=====	=====	=====	=====	=====	=====	=====
	DRAM 1/2 Pitch	180	130	100	70	50	35
	Logic Isol. Lines	140	100	70	50	35	25

We should note that:

- 1) the 1999 column data of the TWG tables should remain the same as the TWG 1998 Update of the 1997 NTRS data;
- 2) the 2002, 2005, 2008, and 2011 column data of the TWG tables should typically be a 1-year "pull-in" of the 1997 NTRS data column headings (2003,6,9,12, respectively); and
- 3) the new 2014 column data can be an extrapolation of the TWG data trend of the 2005-2011 nodes out to one additional 3-year node. [NOTE: for the 1998 Update publication, the 2014 column may apply only to the ORTC Table, since TWGs only committed to review and update their 1997 tables for the nodes 1997,99,01,03,06,09,12 (1999,01,02,05,08,11 for the 1998 Update)].

Similarly, below is the Proposed IRC 1999(b) 2-Year Technology Cycle Header (DRAM Half-pitch-based Nodes, 2-Year Cycle):

Node Header ITEM	ITRS NODE 1999	ITRS NODE 2001	ITRS NODE 2003	ITRS NODE 2005	ITRS NODE 2007	ITRS NODE 2009	ITRS NODE 2011	ITRS NODE 2013	ITRS NODE 2015
=====	=====	=====	=====	=====	=====	=====	=====	=====	=====
DRAM 1/2 Pitch	180	130	100	70	50	35	25	18	12
Logic Isol. Lines	140	100	70	50	35	25	18	12	9
Logic 1/2 Pitch	180	150	115	81	58	41	29	20	14

For the 1999b IRC Proposal, we should note that:

- 1) the 1999 column data of the TWG tables should remain the same as their 1998 Update of the 1997 NTRS data;
- 2) the 2001, 2003, 2005, 2007, and 2009 column data of the TWG tables should typically be the same as that under the 3-year-cycle 1999(b) ITRS data column headings (2002,5,8,11,and 14 respectively); and
- 3) the new 2011,13,15 column data can be generated by extrapolating the TWG 2005-2011 data trends (1997 NTRS 2006-2012) out through 2024, then "capturing" the 3-year cycle data (2017,20,23) and placing it on the 2-year-cycle nodes.
- 4) the new Logic Half-Pitch line item has been added by the IRC and proposed to be typically 15% greater than DRAM Half-Pitch at any given node.

I have used the above guidelines to generate the attached ORTC Tables [1997, 1998/1999(a), 1999(b)].

One additional "word to the wise" - not all line items will lend themselves to extrapolation, so all the TWG table line items will have to be individually reviewed by the TWGs for "common-sense" corrections. As I have mentioned at the Dallas DTWG/RCG meeting, examples of this in the ORTC Table may include:

- 1) Production-level Product Generations. The Japanese IRC representatives have indicated that DRAM will probably remain on a 3-year production introduction for new product generations even if technology accelerates on a 2-year cycle.
Example:

	ITRS		ITRS		ITRS		ITRS		ITRS		ITRS
	NODE		NODE		NODE		NODE		NODE		NODE
Node Header ITEM	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009
=====	=====		=====		=====		=====		=====		=====
DRAM ½ Pitch	180		130		100		70		50		35
Logic Isol. Lines	140		100		70		50		35		25
DRAM Gen. @ Intro.:	1G		4G		16G		64G		256G		1T
DRAM Gen. @ Produc.:	256K			1G		4G				16G	

Obviously, accomodating line item data that does not "fall on" a technology node requires "annualizing" the header. That may require us to limit the published hard copy to 9 years, or change the page orientation to landscape. As mentioned at the Dallas meeting, any data fill-in between nodes will be generated by straight-forward node-to-node interpolation - the TWGs will be responsible only for developing the data which supports the node columns.

- 2) "Affordable" Cost/Function (based on historical product average selling price trends divided by functions per chip). This is a product-market-based roadmap item, originally intended to add a sense of the economic pressures driving the technical roadmap. It is not clear presently what the market impact will be due to accelerating technology. Potential chip size shrink acceleration will lower costs, and thus prices, depending on competition and the supply/demand scenarios of the future. I must develop Inter- and Intra-generation Affordable Cost/Function model scenarios which are consistent with new shrink accelerations.
- 3) Bulk or epitaxial Wafer Diameter. The need for increasing the diameter of the starting material may be delayed if processing technology capability accelerates, since the productivity boost provided by wafer size (historically every 3rd technology generation on 3-year cycle) will be accomplished through die-shrinks instead. This will have to be carefully presented, since the industry will still need wafer-diameter productivity increases if nodes "stretch out" to three-year cycles, after initially accelerating to 2-year cycles.

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
1		INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS															
2		Overall Technology Characteristics Table B-(Rev 1.0m Proposal 12/11/98)															
3		Table B-1 [Multiple Year/Inter-Generation Data]															
4																	
5																	
6		PROPOSED TECHNOLOGY NODE DESIGN RULE:	250				180		130		100			70			50
7		[NEC (Nikkei Microdevices, 9/98)]:	[250]				[180]	[150]	[130]		[100]						
8	WAS (1997) [incl.1998 update, 10/98]	Table Line Item Name															
9	Table Line Item Owner(s):	YEAR OF FIRST PRODUCT SHIPMENT	F'cast 1997	Actual 1997	Model 1998	Actual 1998	1999	Model 2000	2001	Model 2002	2003	Model 2004	Model 2005	2006	Model 2007	Model 2008	2009
10																	
11	Litho TWG	TECHNOLOGY GENERATIONS (nm) DENSE LINES (DRAM Half-Pitch) (nm) WAS	250		212		180	166	153	141	130	119	109	100	89	79	70
12	Litho TWG	TECHNOLOGY GENERATIONS (nm) DENSE LINES (DRAM Half-Pitch) (nm) IS	250		212		180	163	150	136	120	109	99	90	81	72	65
13	Litho TWG	ISOLATED LINES (MPU Gates) (nm) WAS	200		167		140	129	118	109	100	89	79	70	63	56	50
14	Litho TWG	ISOLATED LINES (MPU Gates) (nm) IS	200		167		140	125	115	103	90	81	72	65	58	51	45
15	Litho TWG	Gate Length (nm, post-etch) (NEW LINE ITEM)	200	--	--	--	130	111	100	86	70	63	56	50	44	39	35
16																	
17		Memory															
18	CAG	GENERATION @ samples/introduction	256M			1G	1G	2G		4G				16G			64G
19	CAG	GENERATION @ production ramp	64M			256M	256M	1G		4G				4G			16G
20	CAG	GENERATION @ samples/introduction (bits)	2.7E+08		5.4E+08		1.1E+09	1.5E+09	2.1E+09	3.0E+09	4.3E+09	6.8E+09	1.1E+10	1.7E+10	2.7E+10	4.3E+10	6.9E+10
21	CAG	GENERATION @ production ramp (bits)	6.7E+07		1.3E+08		2.7E+08	3.8E+08	5.4E+08	7.6E+08	1.1E+09	1.7E+09	2.7E+09	4.3E+09	6.8E+09	1.1E+10	1.7E+10
22	CAG	Bits/cm2 @ sample/introduction	9.6E+07		1.6E+08		2.7E+08	3.5E+08	4.6E+08	5.9E+08	7.7E+08	1.1E+09	1.6E+09	2.2E+09	3.1E+09	4.3E+09	6.1E+09
23	CAG	"Affordable" cost/bit @ (packaged - microcents) @ samples/introduction	120		85		60	42	30	21	15	11	7.5	5.3	3.8	2.7	1.9
24		Logic (High-Volume: Microprocessor)															
25	CAG	Logic transistors/cm2 (packaged, including on-chip SRAM)	3.7E+06		4.8E+06		6.2E+06	8.1E+06	1.1E+07	1.4E+07	1.8E+07	2.3E+07	3.0E+07	3.9E+07	5.0E+07	6.5E+07	8.4E+07
26	CAG	Affordable cost/transistor @ (packaged - microcents)	3000		2281		1735	1319	1003	763	580	441	335	255	192.7	145.6	110
27		Logic (Low-Volume: ASIC)															
28	Design TWG	Usable transistors/cm2 (auto layout)	8.0E+06		1.1E+07		1.4E+07	1.6E+07	1.8E+07	2.1E+07	2.4E+07	2.8E+07	3.4E+07	4.0E+07	4.7E+07	5.5E+07	6.4E+07
29	Design TWG	Non-recurring engineering cost/usable transistor (microcents)	50		35		25	22	19	17	15	13	11	10	7.9	6.3	5
30		Number of Chip I/Os															
31	AP/Design TWG	Chip-to-package (pads) high-performance	1450		1703		2000	2213	2400	2656	3000	3302	3634	4000	4421	4886	5400
32	AP/Design TWG	Chip-to-package (pads) cost-performance	800		883		975	1079	1195	1322	1460	1613	1783	1970	2176	2404	2655
33		Number of Package Pins/Balls															
34	AP/Design TWG	Microprocessor/controller, cost-performance	600		697		810	874	900	972	1100	1220	1353	1500	1651	1817	2000
35	AP/Design TWG	ASIC (high-performance)	1100		1285		1500	1651	1800	1981	2200	2440	2705	3000	3329	3695	4100
36		Cost-Per-Pin															
37	AP TWG	Package cost (cents/pin) (cost-performance) - maximum	2.80		2.52		2.27	2.16	2.05	1.95	1.86	1.77	1.68	1.59	1.51	1.44	1.37
38	AP TWG	Package cost (cents/pin) (cost-performance) - minimum	1.40		1.21		1.04	0.98	0.94	0.89	0.83	0.80	0.76	0.73	0.70	0.66	0.63
39	Genda Hu/ERSO	Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)			1.00		0.90	0.80	0.80	0.80							
40		Chip Frequency (MHz)															
41	Design TWG	On-chip local clock, (high performance)	750		968		1250	1423	1500	1708	2100	2490	2952	3500	4189	5013	6000
42	Design TWG	On-chip, across-chip clock (high performance)	750		949		1200	1289	1400	1504	1600	1724	1857	2000	2154	2321	2500
43	Design TWG	On-chip, across-chip clock, high-performance ASIC (new line item)	300		387		500	544	600	653	700	761	828	900	991	1090	1200
44	Design, TWG	On-chip, across-chip clock (cost-performance)	400		490		600	645	700	752	800	890	989	1100	1192	1292	1400
45																	
46	Design TWG	Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)	750		949		1200	1289	1400	1504	1600	1724	1857	2000	2154	2321	2500
47		Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	250		346		480	559	785	915	885	932	982	1035	1112	1196	1285
48		Chip Size (mm2) (@ sample/introduction)															
49	CAG	DRAM	280		335	569	400	435	445	484	560	628	704	790	887	997	1120
50	CAG	Microprocessor	300		319		340	361	385	408	430	458	488	520	551	585	620
51	Des. TWG/PIDS	ASIC [max litho field area]	480		620		800	824	850	875	900	932	965	1000	1032	1066	1100
52																	
53	Litho TWG	Maximum Lithographic Field Size - Area (mm2)	484		622		800	824	850	875	900	932	965	1000	1032	1066	1100
54	Litho TWG	Maximum Lithographic Field Size - Width (mm)	22		27		32	33	34	35	36	37	39	40	41	43	44
55	Litho TWG	Maximum Lithographic Field Size - Length (mm)	22		23		25	25	25	25	25	25	25	25	25	25	25
56	Interconnect TWG, PIDS	Maximum Number Wiring Levels - maximum	6		6		6	7	7	7	7	7	8	8	8	9	9
57	Interconnect TWG, PIDS	Maximum Number Wiring Levels - minimum	6		6		6	6	7	7	7	7	7	7	7	8	8
58		Defect Reduction															
59	Defect Reduc. Technol. TWG	DRAM 1st Year Electrical DO @ 60% Yield (d/m2)	2080		1740		1455	1338	1310	1205	1040	926	825	735	655	584	520
60	Defect Reduc. Technol. TWG	DRAM 3rd Year Electrical DO @ 80% Yield (d/m2)	1390		1170		985	903	875	802	695	619	551	490	438	392	350
61	Defect Reduc. Technol. TWG	MPU 1st Year Electrical DO @ 60% Yield (d/m2)	1940		1821		1710	1613	1510	1425	1355	1272	1193	1120	1056	997	940
62	Defect Reduc. Technol. TWG	MPU 3rd Year Electrical DO @ 80% Yield (d/m2)	1310		1227		1150	1085	1025	967	910	857	807	760	718	678	640
63	Defect Reduc. Technol. TWG	ASIC 1st Year Electrical DO @ 60% Yield (d/m2)	1210		937		725	704	685	665	645	623	601	580	563	546	530
64																	
65	PIDS	Minimum, mask count - maximum	22		23		24	24	23	23	24	25	25	26	27	27	28
66	PIDS	Minimum, mask count - minimum	22		22		22	22	23	24	24	24	24	24	25	25	26
67		Maximum substrate diameter (mm)															
68	CAG, FI, I300I	Bulk or epitaxial or SOI** wafer	200		200		300	300	300	300	300	300	300	300	300	300	450
69		Power Supply Voltage (V)															
70	PIDS	Minimum logic Vdd (V) - maximum [for maximum performance]	2.5		2.1		1.8	1.7	1.5	1.4	1.5	1.4	1.3	1.2	1.1	1.0	0.9
71	PIDS	Minimum logic Vdd (V) - minimum [for lowest power]	1.8		1.7		1.6	1.5	1.2	1.1	1.2	1.1	1.0	0.9	0.79	0.69	0.6
72		Maximum Power															
73	AP TWG	High-performance with heatsink (W)	70		79		90	99	110	121	130	139	149	160	163	167	170
74	AP TWG	Battery (W) - (Hand-held)	1.2		1.3		1.4	1.5	1.7	1.9	2.0	2.1	2.3	2.4	2.5	2.7	2.8
75		Test															
76	Test TWG	Volume tester cost/pin (\$K/pin) (high-performance)	10		9		8	7	7	7	6	6	5	5	5	5	5
77	Test TWG	Volume tester cost/pin (\$K/pin) (cost-performance)	5		4		4	4	3	3	3	3	2	2	2	2	2
78																	
79																	
80		***Silicon On Insulator															

	A	B	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG
1		INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS																
2		Overall Technology Characteristics Table B-(Rev 1.0m Proposal 12/11/98)																
3		Table B-1 [Multiple Year/Inter-Generation Data]																
4																		
5																		
6		PROPOSED TECHNOLOGY NODE DESIGN RULE:			35			25										
7		[NEC (Nikkei Microdevices, 9/98)]:																
8	WAS (1997) [incl.1998 update, 10/98]	Table Line Item Name								Trend	Trend	Trend	Trend	Trend	Trend	Trend	Trend	Trend
9	Table Line Item Owner(s):	YEAR OF FIRST PRODUCT SHIPMENT	Model	Model	2012	Model	Model	Model		'97-'99	'97-'12	'03-'12	'99-'03	'99-'01	'01-'03	'03-'06	'06-'09	'09-'12
10			2010	2011		2013	2014	2015		CAGR	CAGR	CAGR	CAGR	CAGR	CAGR	CAGR	CAGR	
11	Litho TWG	TECHNOLOGY GENERATIONS (nm) DENSE LINES (DRAM Half-Pitch) (nm)WAS	63	56	50	45	40	36		-15.1%	-10.2%	-10.1%	-7.8%	-7.8%	-7.8%	-8.4%	-11.2%	-10.6%
12	Litho TWG	TECHNOLOGY GENERATIONS (nm) DENSE LINES (DRAM Half-Pitch) (nm) IS	58	51	45	40	36	32		-15.1%	-10.8%	-10.3%	-9.6%	-8.7%	-10.6%	-9.1%	-10.3%	-11.5%
13	Litho TWG	ISOLATED LINES (MPU Gates) (nm) WAS	45	40	35	32	28	25		-16.3%	-10.9%	-10.9%	-8.1%	-8.1%	-8.1%	-11.2%	-10.6%	-10.9%
14	Litho TWG	ISOLATED LINES (MPU Gates) (nm) IS	39	34	30	27	24	21		-16.3%	-11.9%	-11.9%	-10.5%	-9.4%	-11.5%	-10.3%	-11.5%	-12.6%
15	Litho TWG	Gate Length (nm, post-etch) (NEW LINE ITEM)	31	28	25	22	20	18		-19.4%	-12.9%	-10.8%	-14.3%	-12.3%	-16.3%	-10.6%	-11.2%	-10.6%
16																		
17		Memory																
18	CAG	GENERATION @ samples/introduction			256G			1T										
19	CAG	GENERATION @ production ramp			64G			256G										
20	CAG	GENERATION @ samples/introduction (bits)	1.1.E+11	1.7.E+11	2.7E+11	4.4E+11	6.9E+11	1.1E+12		100.0%	58.7%	58.7%	41.4%	41.4%	41.4%	58.7%	58.7%	58.7%
21	CAG	GENERATION @ production ramp (bits)	2.7.E+10	4.3.E+10	6.9E+10	1.1E+11	1.7E+11	2.7E+11		100.0%	58.7%	58.7%	41.4%	41.4%	41.4%	58.7%	58.7%	58.7%
22	CAG	Bits/cm2 @ sample/introduction	8.6.E+09	1.2.E+10	1.7E+10	2.4E+10	3.4E+10	4.8E+10		67.7%	41.3%	41.2%	30.0%	30.0%	30.0%	41.9%	40.5%	41.2%
23	CAG	"Affordable" cost/bit @ (packaged - microcents) @ samples/introduction	1.3	0.9	0.66	0.47	0.33	0.23		-29.3%	-29.3%	-29.3%	-29.3%	-29.3%	-29.3%	-29.3%	-29.0%	-29.7%
24		Logic (High-Volume: Microprocessor)																
25	CAG	Logic transistors/cm2 (packaged, including on-chip SRAM)	1.1.E+08	1.4.E+08	1.8E+08	2.3E+08	3.0E+08	3.9E+08		29.4%	29.6%	29.2%	30.5%	30.5%	29.4%	29.1%	28.9%	28.9%
26	CAG	Affordable cost/transistor @ (packaged - microcents)	84.6	65.0	50	38	29	22		-24.0%	-23.9%	-23.8%	-24.0%	-24.0%	-24.0%	-24.4%	-23.1%	-23.1%
27		Logic (Low-Volume: ASIC)																
28	Design TWG	Usable transistors/cm2 (auto layout)	7.4.E+07	8.6.E+07	1.0E+08	1.2E+08	1.4E+08	1.6E+08		32.3%	18.3%	17.2%	14.4%	14.4%	14.4%	18.6%	17.0%	16.0%
29	Design TWG	Non-recurring engineering cost/usable transistor (microcents)	4.0	3.1	2.5	2.0	1.7	1.4		-29.3%	-18.1%	-18.1%	-12.0%	-12.0%	-12.0%	-20.6%	-20.6%	-20.6%
30		Number of Chip I/Os																
31	AP/Design TWG	Chip-to-package (pads) high-performance	5971	6602	7300	8058	8895	9819		17.4%	11.4%	10.4%	10.7%	9.5%	11.8%	10.1%	10.5%	10.6%
32	AP/Design TWG	Chip-to-package (pads) cost-performance	2935	3244	3585	3961	4377	4837		10.4%	10.5%	10.5%	10.6%	10.7%	10.5%	10.5%	10.5%	10.5%
33		Number of Package Pins/Balls																
34	AP/Design TWG	Microprocessor/controller, cost-performance	2210	2443	2700	2983	3296	3642		16.2%	10.5%	10.5%	8.0%	5.4%	10.6%	10.9%	10.1%	10.5%
35	AP/Design TWG	ASIC (high-performance)	4522	4987	5500	6089	6742	7465		16.8%	11.3%	10.7%	10.0%	9.5%	10.6%	10.9%	11.0%	10.3%
36		Cost-Per-Pin																
37	AP TWG	Package cost (cents/pin) (cost-performance) -maximum	1.30	1.23	1.17	1.11	1.06	1.00		-10.0%	-5.7%	-5.0%	-4.9%	-5.0%	-4.7%	-5.1%	-4.8%	-5.1%
38	AP TWG	Package cost (cents/pin) (cost-performance) - minimum	0.60	0.57	0.54	0.51	0.49	0.47		-13.8%	-6.2%	-4.7%	-5.5%	-4.9%	-6.0%	-4.2%	-4.8%	-5.0%
39	Genda Hu/ERSO	Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)								N/A	N/A	N/A	N/A	-5.7%	N/A	N/A	N/A	N/A
40		Chip Frequency (MHz)																
41	Design TWG	On-chip local clock, (high performance)	7114	8434	10000	11893	14145	16824		29.1%	18.8%	18.9%	13.8%	9.5%	18.3%	18.6%	19.7%	18.6%
42	Design TWG	On-chip, across-chip clock (high performance)	2657	2823	3000	3217	3450	3699		26.5%	9.7%	7.2%	7.5%	8.0%	6.9%	7.7%	7.7%	6.3%
43	Design TWG	On-chip, across-chip clock, high-performance ASIC (new line item)	1293	1392	1500	1633	1777	1934		29.1%	11.3%	8.8%	8.8%	9.5%	8.0%	8.7%	10.1%	7.7%
44	Design, TWG	On-chip, across-chip clock (cost-performance)	1522	1655	1800	1970	2155	2359		22.5%	10.5%	9.4%	7.5%	8.0%	6.9%	11.2%	8.4%	8.7%
45																		
46	Design TWG	Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)	2657	2823	3000	3217	3450	3699		26.5%	9.7%	7.2%	7.5%	8.0%	6.9%	7.7%	7.7%	6.3%
47		Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	1365	1450	1540	1638	1742	1852		38.6%	12.9%	6.3%	16.5%	27.9%	6.2%	5.4%	7.5%	6.2%
48		Chip Size (mm2) (@ sample/introduction)																
49	CAG	DRAM	1256	1409	1580	1773	1990	2233		19.5%	12.2%	12.2%	8.8%	5.5%	12.2%	12.2%	12.3%	12.2%
50	CAG	Microprocessor	661	704	750	798	849	903		6.5%	6.3%	6.4%	6.0%	6.4%	5.7%	6.5%	6.0%	6.6%
51	Des. TWG/PIDS	ASIC [max litho field area]	1163	1230	1300	1354	1411	1470		29.1%	6.9%	4.2%	3.0%	3.1%	2.9%	3.6%	3.2%	5.7%
52																		
53	Litho TWG	Maximum Lithographic Field Size - Area (mm2)	1163	1230	1300	1354	1411	1470		28.6%	6.8%	4.2%	3.0%	3.1%	2.9%	3.6%	3.2%	5.7%
54	Litho TWG	Maximum Lithographic Field Size - Width (mm)	47	49	52	54	56	59		20.6%	5.9%	4.2%	3.0%	3.1%	2.9%	3.6%	3.2%	5.7%
55	Litho TWG	Maximum Lithographic Field Size - Length (mm)	25	25	25	25	25	25		6.6%	0.9%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
56	Interconnect TWG, PIDS	Maximum Number Wiring Levels - maximum	9	9	9	9	10	10		8.0%	2.7%	2.8%	0.0%	0.0%	4.6%	4.0%	4.0%	4.0%
57	Interconnect TWG, PIDS	Maximum Number Wiring Levels - minimum	8	9	9	9	10	10		0.0%	2.7%	2.8%	3.9%	8.0%	0.0%	0.0%	4.6%	4.0%
58		Defect Reduction																
59	Defect Reduc. Technol. TWG	DRAM 1st Year Electrical DO @ 60% Yield (d/m2)	464	414	370	330	294	262		-16.4%	-10.9%	-10.8%	-8.1%	-5.1%	-10.9%	-10.9%	-10.9%	-10.7%
60	Defect Reduc. Technol. TWG	DRAM 3rd Year Electrical DO @ 80% Yield (d/m2)	313	280	250	223	199	176		-15.8%	-10.8%	-10.7%	-8.3%	-5.7%	-10.9%	-11.0%	-10.6%	-10.6%
61	Defect Reduc. Technol. TWG	MPU 1st Year Electrical DO @ 60% Yield (d/m2)	881	827	775	728	685	643		-6.1%	-5.9%	-6.0%	-5.7%	-6.0%	-5.3%	-6.2%	-5.7%	-6.2%
62	Defect Reduc. Technol. TWG	MPU 3rd Year Electrical DO @ 80% Yield (d/m2)	599	561	525	494	465	437		-6.3%	-5.9%	-5.9%	-5.7%	-5.6%	-5.8%	-5.8%	-5.6%	-6.4%
63	Defect Reduc. Technol. TWG	ASIC 1st Year Electrical DO @ 60% Yield (d/m2)	502	475	450	432	415	399		-22.6%	-6.4%	-3.9%	-2.9%	-2.8%	-3.0%	-3.5%	-3.0%	-5.3%
64																		
65	PIDS	Minimum, mask count - maximum	28	28	28	28	29	29		4.4%	1.6%	1.7%	0.0%	-2.1%	2.2%	2.7%	2.5%	0.0%
66	PIDS	Minimum, mask count - minimum	27	27	28	28	29	29		0.0%	1.6%	1.7%	2.2%	2.2%	2.2%	0.0%	2.7%	2.5%
67		Maximum substrate diameter (mm)																
68	CAG, FI, I300I	Bulk or epitaxial or SOI** wafer	450	450	450	450	450	450		22.5%	5.6%	4.6%	0.0%	0.0%	0.0%	0.0%	14.5%	0.0%
69		Power Supply Voltage (V)																
70	PIDS	Minimum logic Vdd (V) - maximum [for maximum performance]	0.79	0.69	0.60	0.54	0.49	0.44		-15.1%	-9.1%	-9.7%	-4.5%	-8.7%	0.0%	-7.2%	-9.1%	-12.6%
71	PIDS	Minimum logic Vdd (V) - minimum [for lowest power]	0.56	0.53	0.50	0.45	0.41	0.37		-6.3%	-8.2%	-9.3%	-6.6%	-12.9%	0.0%	-9.1%	-12.6%	-5.9%
72		Maximum Power																
73	AP TWG	High-performance with heatsink (W)	172	173	175	181	187	193		13.4%	6.3%	3.4%	9.6%	10.6%	8.7%	7.2%	2.0%	1.0%
74	AP TWG	Battery (W) - (Hand-held)	2.9	3.1	3.2	3	4	4		8.0%	6.8%	5.4%	9.3%	10.2%	8.5%	6.3%	5.	

	A	B	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF																		
1		INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS																																	
2		Overall Technology Characteristics Table B-1 [Rev 3.0b IRC Proposal 12/11/98]																																	
3		Table B-1 [Multiple Year Inter-Generation Data]																																	
4																																			
5																																			
6		PROPOSED TECHNOLOGY NODE DESIGN RULE:		50			35			25			18			12																			
7		[NEC (Nikkei Microdevices, 9/98)]:																																	
8	Proposed (1998, 1999a) [incl.1998 update, 10/98]	Table Line Item Name:																																	
9	Table Line Item Owner(s):	YEAR OF FIRST PRODUCT SHIPMENT IS [WAS]	Model	2010	2011[12]	Model	2012	Model	2013	Model	2014[15]	Model	2015	Model	2016	Model	2017[18]	Model	2018	Model	2019	Model	2020[21]	Model	2021	Model	2022	Model	2023[24]	Model	2024				
10																																			
11	Litho TWG	TECHNOLOGY GENERATIONS (nm)																																	
12	Litho TWG	DENSE LINES (DRAM Half-Pitch) WAS	56	50		45	40	35	31	28	25	22	20	18	16	14	13	11																	
13	Litho TWG	TECHNOLOGY GENERATIONS (nm)																																	
14	Litho TWG	ISOLATED LINES (Logic Gates) WAS	39	35		31	28	25	22	20	18	16	14	12	11	10	9	8																	
15	Litho TWG	TECHNOLOGY GENERATIONS (nm)																																	
16	Litho TWG	ISOLATED LINES (Logic Gates) IS																																	
17	Litho TWG	Gate Length (nm, post-etch)(NEW LINE ITEM) WAS																																	
18	Litho TWG	Gate Length (nm, post-etch)(NEW LINE ITEM) IS [REMOVE LINE ITEM]																																	
19	CAG	Memory																																	
20	CAG	GENERATION @ samples/introduction		256G							1T						4T																		
21	CAG	GENERATION @ production ramp		64G							256G						1T																		
22	CAG	GENERATION @ samples/introducer (bits)	1.7E+11	2.7E+11	4.4E+11	6.9E+11	1.1E+12	1.7E+12	2.8E+12	4.4E+12	7.0E+12	1.1E+13	1.8E+13	2.8E+13	4.4E+13	7.0E+13	1.1E+14	1.8E+14	2.8E+14	4.4E+14	7.0E+14	1.1E+15	1.8E+15	2.8E+15	4.4E+15	7.0E+15	1.1E+16	1.8E+16	2.8E+16	4.4E+16	7.0E+16	1.1E+17			
23	CAG	GENERATION @ production ramp (bits)	4.3E+10	6.9E+10	1.1E+11	1.7E+11	2.7E+11	4.4E+11	6.9E+11	1.1E+12	1.7E+12	2.8E+12	4.4E+12	7.0E+12	1.1E+13	1.8E+13	2.8E+13	4.4E+13	7.0E+13	1.1E+14	1.8E+14	2.8E+14	4.4E+14	7.0E+14	1.1E+15	1.8E+15	2.8E+15	4.4E+15	7.0E+15	1.1E+16	1.8E+16	2.8E+16	4.4E+16		
24	CAG	Bits/cm2 @ sample/introduction	1.2E+10	1.7E+10	2.4E+10	3.4E+10	4.8E+10	6.8E+10	9.5E+10	1.3E+11	1.9E+11	2.7E+11	3.7E+11	5.3E+11	7.4E+11	1.0E+12	1.4E+12	1.9E+12	2.7E+12	3.7E+12	5.3E+12	7.4E+12	1.0E+13	1.4E+13	1.9E+13	2.7E+13	3.7E+13	5.3E+13	7.4E+13	1.0E+14	1.4E+14	1.9E+14			
25	CAG	*Affordable* cost/bit @ (packaged - microcents) @ samples/introduction	0.94	0.66	0.47	0.33	0.23	0.16	0.12	0.082	0.058	0.041	0.029	0.020	0.014	0.010	0.007																		
26	CAG	Logic (High-Volume: Microprocessor)																																	
27	CAG	Logic transistors/cm2 (packed, including on-chip SRAM)	1.4E+08	1.8E+08	2.3E+08	3.0E+08	3.9E+08	5.0E+08	6.4E+08	8.3E+08	1.1E+09	1.4E+09	1.8E+09	2.3E+09	3.0E+09	3.8E+09	4.9E+09																		
28	CAG	Affordable cost/transistor @ (packaged - microcents)	65	50	38	29	22	17	13	10	7.5	5.7	4.3	3.3	2.5	1.9	1.5																		
29	CAG	Logic (Low-Volume: ASIC)																																	
30	Design TWG	Usable transistors/cm2 (auto layout)	8.6E+07	1.0E+08	1.2E+08	1.4E+08	1.6E+08	1.8E+08	2.1E+08	2.5E+08	2.9E+08	3.4E+08	4.0E+08	4.6E+08	5.4E+08	6.3E+08	7.3E+08																		
31	Design TWG	Non-recurring engineering cost/usable transistor (microcents)	3.1	2.5	2.0	1.6	1.3	1.0	0.79	0.63	0.50	0.39	0.31	0.25	0.20	0.16	0.12																		
32	AP/Design TWG	Chip-to-package (pads) high-performance	6602	7300	8070	8921	9862	10902	12052	13323	14728	16281	17998	19896	21994	24314	26878																		
33	AP/Design TWG	Chip-to-package (pads) cost-performance	3244	3585	3961	4377	4836	5344	5904	6524	7209	7965	8801	9724	10745	11872	13118																		
34	AP/Design TWG	Number of Package Pins/Balls																																	
35	AP/Design TWG	Microprocessor/controller, cost-performance	2443	2700	2978	3284	3622	3995	4406	4860	5360	5912	6520	7191	7932	8748	9648																		
36	AP/Design TWG	ASIC (high-performance)	4987	5500	6085	6731	7447	8239	9114	10083	11155	12341	13653	15104	16710	18486	20451																		
37	AP TWG	Cost-Per-Pin																																	
38	AP TWG	Package cost (cents/pin) (cost-performance) - maximum	1.23	1.17	1.11	1.06	1.00	0.95	0.91	0.86	0.82	0.78	0.74	0.70	0.67	0.63	0.60																		
39	AP TWG	Package cost (cents/pin) (cost-performance) - minimum	0.57	0.54	0.51	0.49	0.46	0.44	0.42	0.40	0.38	0.36	0.34	0.33	0.31	0.30	0.28																		
40	Genda Hu/ERSO	Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)																																	
41	Design TWG	Chip Frequency (MHz)																																	
42	Design TWG	On-chip local clock, (high performance)	8434	10000	11912	14190	16903	20135	23985	28571	34035	40542	48295	57529	68529	81633	97242																		
43	Design TWG	On-chip, across-chip clock (high performance)	2823	3000	3210	3434	3674	3931	4206	4500	4815	5151	5511	5897	6309	6750	7222																		
44	Design TWG	On-chip, across-chip clock, high-performance ASIC (new line item)	1392	1500	1633	1778	1936	2109	2296	2500	2722	2964	3227	3514	3827	4167	4537																		
45	Design TWG	On-chip, across-chip clock (cost-performance)	1655	1800	1954	2121	2303	2500	2713	2945	3197	3471	3768	4090	4440	4820	5232																		
46	Design TWG	Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)	2823	3000	3210	3434	3674	3931	4206	4500	4815	5151	5511	5897	6309	6750	7222																		
47	Design TWG	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	1450	1540	1645	1758	1878	2007	2145	2291	2448	2616	2795	2986	3191	3409	3643																		
48	Design TWG	Chip Size (mm2) (@ sample/introduction)																																	
49	CAG	DRAM	1409	1580	1773	1991	2234	2508	2815	3160	3547	3981	4469	5016	5630	6320	7094																		
50	CAG	Microprocessor	704	750	797	847	901	957	1018	1082	1150	1222	1299	1381	1468	1560	1658																		
51	Des. TWG/PIDS	ASIC [max litho field area]	1230	1300	1358	1419	1482	1548	1618	1690	1766	1844	1927	2013	2103	2197	2295																		
52	Design TWG	Maximum Lithographic Field Size - Area (mm2)	1230	1300	1358	1419	1482	1548	1618	1690	1766	1844	1927	2013	2103	219																			

	A	B	AG	AH	AI	AJ	AK	AL	AM	AN	AO	AP
1		INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS										
2		Overall Technology Characteristics Table B-1 (Rev 3.0b IRC Proposal 12/11/98)										
3		Table B-1 [Multiple Year Inter-Generation Data]										
4												
5												
6		PROPOSED TECHNOLOGY NODE DESIGN RULE:										
7		[NEC (Nikkei Microdevices, 9/98)]:										
8	Proposed (1998, 1999a) [incl.1998 update, 10/98]	Table Line Item Name:	Model 2025	Trend '97-'99	Trend '99-'14	Trend ['03-'12] '05-'11	Trend '99-'02	Trend ['03-'06] '02-'05	Trend ['06-'09] '05-'08	Trend ['09-'12] '08-'11	Trend ['12-'15] '11-'14	
9	Table Line Item Owner(s):	YEAR OF FIRST PRODUCT SHIPMENT IS (WAS)		CAGR	CAGR	CAGR	CAGR	CAGR	CAGR	CAGR	CAGR	
10												
11	Litho TWG	TECHNOLOGY GENERATIONS (nm)	DENSE LINES (DRAM Half-Pitch) WAS	10	-15.1%	-10.3%	-10.9%	-10.3%	-8.4%	-11.2%	-10.6%	-10.9%
12	Litho TWG	TECHNOLOGY GENERATIONS (nm)	DENSE LINES (DRAM Half-Pitch) IS									
13	Litho TWG	TECHNOLOGY GENERATIONS (nm)	ISOLATED LINES (Logic Gates) WAS	7	-16.3%	-10.9%	-10.9%	-10.6%	-11.2%	-10.6%	-11.2%	-10.9%
14	Litho TWG	TECHNOLOGY GENERATIONS (nm)	ISOLATED LINES (Logic Gates) IS									
15	Litho TWG	Gate Length (nm, post-etch)(NEW LINE ITEM) WAS										
16	Litho TWG	Gate Length (nm, post-etch)(NEW LINE ITEM) IS (REMOVE LINE ITEM)										
17		Memory										
18	CAG	GENERATION @ samples/introduction										
19	CAG	GENERATION @ production ramp										
20	CAG	GENERATION @ samples/introducer (bits)	1.8E+14	100.0%	58.7%	58.7%	58.7%	58.7%	58.7%	58.7%	58.7%	58.7%
21	CAG	GENERATION @ production ramp (bits)	4.4E+13	100.0%	58.7%	58.7%	58.7%	58.7%	58.7%	58.7%	58.7%	58.7%
22	CAG	Bits/cm2 @ sample/introduction	2.1E+12	67.7%	41.3%	40.9%	41.8%	41.9%	40.5%	41.2%	40.9%	40.9%
23	CAG	*Affordable* cost/bit @ (packaged - microcents) @ samples/introduction	0.005	-42.3%	-29.0%	-29.3%	-27.9%	-29.3%	-29.0%	-29.7%	-29.3%	-29.3%
24		Logic (High-Volume: Microprocessor)										
25	CAG	Logic transistors/cm2 (packed, including on-chip SRAM)	6.4E+09	29.4%	31.7%	29.0%	42.7%	29.4%	29.1%	28.9%	29.0%	29.0%
26	CAG	Affordable cost/transistor @ (packaged - microcents)	1.1	-24.0%	-25.2%	-23.8%	-30.6%	-24.0%	-24.4%	-23.1%	-23.8%	-23.8%
27		Logic (Low-Volume: ASIC)										
28	Design TWG	Usable transistors/cm2 (auto layout)	8.5E+08	32.3%	17.5%	16.5%	19.7%	18.6%	17.0%	16.0%	16.5%	16.5%
29	Design TWG	Non-recurring engineering cost/usable transistor (microcents)	0.10	-29.3%	-18.1%	-20.6%	-15.7%	-12.6%	-20.6%	-20.6%	-20.6%	-20.6%
30		Number of Chip I/Os										
31	AP/Design TWG	Chip-to-package (pads) high-performance	29712	17.4%	11.2%	10.5%	14.5%	10.1%	10.5%	10.6%	10.5%	10.5%
32	AP/Design TWG	Chip-to-package (pads) cost-erformance	14495	10.4%	11.3%	10.5%	14.4%	10.5%	10.5%	10.5%	10.5%	10.5%
33		Number of Package Pins/Balls										
34	AP/Design TWG	Microprocessor/controller, cost-performance	10641	16.2%	10.5%	10.3%	10.7%	10.9%	10.1%	10.5%	10.3%	10.3%
35	AP/Design TWG	ASIC (high-performance)	22625	16.8%	11.3%	10.6%	13.6%	10.9%	11.0%	10.3%	10.6%	10.6%
36		Cost-Per-Pin										
37	AP TWG	Package cost (cents/pin) (cost-performance) - maximum	0.57	-10.0%	-5.3%	-5.0%	-6.4%	-5.1%	-4.8%	-5.1%	-5.0%	-5.0%
38	AP TWG	Package cost (cents/pin) (cost-performance) - minimum	0.27	-13.8%	-5.2%	-4.9%	-7.2%	-4.2%	-4.8%	-5.0%	-4.9%	-4.9%
39	Genda Hu/ERSO	Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)		N/A	N/A	N/A	-3.9%	N/A	N/A	N/A	N/A	N/A
40		Chip Frequency (MHz)										
41	Design TWG	On-chip local clock, (high performance)	115835	29.1%	19.0%	19.1%	18.9%	18.6%	19.7%	18.6%	19.1%	19.1%
42	Design TWG	On-chip, across-chip clock (high performance)	7727	26.5%	7.7%	7.0%	10.1%	7.7%	7.7%	6.3%	7.0%	7.0%
43	Design TWG	On-chip, across-chip clock, high-performance ASIC (new line item)	4940	29.1%	9.4%	8.9%	11.9%	8.7%	10.1%	7.7%	8.9%	8.9%
44	Design, TWG	On-chip, across-chip clock (cost-performance)	5680	22.5%	9.4%	8.6%	10.1%	11.2%	8.4%	8.7%	8.6%	8.6%
45												
46	Design TWG	Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)	7727	26.5%	7.7%	7.0%	10.1%	7.7%	7.7%	6.3%	7.0%	7.0%
47		Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	3892	38.6%	9.5%	6.8%	22.6%	5.4%	7.5%	6.2%	6.8%	6.8%
48		Chip Size (mm2) (@sample/introduction)										
49	CAG	DRAM	7963	19.5%	12.2%	12.2%	11.9%	12.2%	12.3%	12.2%	12.2%	12.2%
50	CAG	Microprocessor	1763	6.5%	6.7%	6.3%	8.1%	6.5%	6.0%	6.6%	6.3%	6.3%
51	Des. TWG/PIDS	ASIC [max litho field area]	2398	29.1%	4.2%	4.5%	4.0%	3.6%	3.2%	5.7%	4.5%	4.5%
52												
53	Litho TWG	Maximum Lithographic Field Size - Area (mm2)	2398	28.6%	4.2%	4.5%	4.0%	3.6%	3.2%	5.7%	4.5%	4.5%
54	Litho TWG	Maximum Lithographic Field Size - Width (mm)	96	20.6%	4.2%	4.5%	4.0%	3.6%	3.2%	5.7%	4.5%	4.5%
55	Litho TWG	Maximum Lithographic Field Size - Length (mm)	25	6.6%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
56	Interconnect TWG, PIDS	Maximum Number Wiring Levels - maximum	12	8.0%	2.1%	2.0%	0.0%	4.6%	4.0%	0.0%	2.0%	2.0%
57	Interconnect TWG, PIDS	Maximum Number Wiring Levels - minimum	16	0.0%	3.6%	4.3%	5.3%	0.0%	4.6%	4.0%	4.3%	4.3%
58		Defect Reduction										
59	Defect Reduc.Technol.TWG	DRAM 1st Year Electrical DO @ 60% Yield (d/m2)	75	-16.4%	-10.8%	-10.8%	-10.6%	-10.9%	-10.9%	-10.7%	-10.8%	-10.8%
60	Defect Reduc.Technol.TWG	DRAM 3rd Year Electrical DO @ 80% Yield (d/m2)	52	-15.8%	-10.8%	-10.6%	-11.0%	-11.0%	-10.6%	-10.6%	-10.6%	-10.6%
61	Defect Reduc.Technol.TWG	MPU 1st Year Electrical DO @ 60% Yield (d/m2)	328	-6.1%	-6.3%	-6.0%	-7.5%	-6.2%	-5.7%	-6.2%	-6.0%	-6.0%
62	Defect Reduc.Technol.TWG	MPU 3rd Year Electrical DO @ 80% Yield (d/m2)	221	-6.3%	-6.3%	-6.0%	-7.5%	-5.8%	-5.6%	-6.4%	-6.0%	-6.0%
63	Defect Reduc.Technol.TWG	ASIC 1st Year Electrical DO @ 60% Yield (d/m2)	249	-22.6%	-3.9%	-4.1%	-3.8%	-3.5%	-3.0%	-5.3%	-4.1%	-4.1%
64												
65	PIDS	Minimum, mask count - maximum	33	4.4%	1.3%	1.2%	0.0%	2.7%	2.5%	0.0%	1.2%	1.2%
66	PIDS	Minimum, mask count - minimum	40	0.0%	2.1%	2.6%	2.9%	0.0%	2.7%	2.5%	2.6%	2.6%
67		Maximum substrate diameter (mm)										
68	CAG, FI, I300I	Bulk or epitaxial or SOI*** wafer	675	4.6%	4.6%	4.6%	4.6%	4.6%	4.6%	4.6%	4.6%	4.6%
69		Power Supply Voltage (V)										
70	PIDS	Minimum logic Vdd (V) - maximum [for maximum performance]	0.12	-15.1%	-9.2%	-10.9%	-5.9%	-7.2%	-9.1%	-12.6%	-10.9%	-10.9%
71	PIDS	Minimum logic Vdd (V) - minimum [for lowest power]	0.13	-6.3%	-9.2%	-9.3%	-8.8%	-9.1%	-12.6%	-5.9%	-9.3%	-9.3%
72		Maximum Power										
73	AP TWG	High-performance with heatsink (W)	216	13.4%	4.8%	1.5%	13.0%	7.2%	2.0%	1.0%	1.5%	1.5%
74	AP TWG	Battery (W) - (Hand-held)	6.3	8.0%	6.7%	4.9%	12.6%	6.3%	5.3%	4.6%	4.9%	4.9%
75		Test										
76	Test TWG	Volume tester cost/pin (\$K/pin) (high-performance)	5	-10.6%	-3.1%	0.0%	-9.1%	-5.9%	0.0%	0.0%	0.0%	0.0%
77	Test TWG	Volume tester cost/pin (\$K/pin) (cost-performance)	2	-10.6%	-4.5%	0.0%	-9.1%	-12.6%	0.0%	0.0%	0.0%	0.0%
78												
79												
80		***Silicon On Insulator										

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
1		INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS															
2		Overall Technology Characteristics Table B-1(Rev 2.3f IRC Proposal 11/30/98)															
3		Table B-1 [Multiple Year/Inter-Generation Data]															
4																	
5																	
6		PROPOSED TECHNOLOGY NODE DESIGN RULE:	250				180		130		100		70		50		35
7		[NEC (Nikkei Microdevices, 9/98)]:	[250]				[180]	[150]	[130]		[100]						
8	Proposed [1999b - (2yr)] [incl.1998 update, 10/98]	Table Line Item Name:															
9	Table Line Item Owner(s):	YEAR OF FIRST PRODUCT SHIPMENT	F'cast 1997	Actual 1997	Model 1998	Actual 1998	1999	Model 2000	2001[02]	Model 2002	2003[05]	Model 2004	2005[08]	Model 2006	2007[11]	Model 2008	2009[14]
10	Litho TWG	TECHNOLOGY GENERATIONS (nm) DENSE LINES (DRAM Half-Pitch)	250		212		180	153	130	114	100	84	70	59	50	42	35
11	Litho TWG	TECHNOLOGY GENERATIONS (nm) ISOLATED LINES (Logic Gates)	200		167		140	118	100	84	70	59	50	42	35	29	25
12	TBD	TECHNOLOGY GENERATIONS (nm) Logic Half-Pitch	N/A		N/A		180	164	150	131	115	96	81	68	58	48	41
13		Memory															
14	CAG	GENERATION @ samples/introducer (2-Year Introduction Cycle)	256M			1G	1G	2G	4G	8G	16G	32G	64G	128G	256G	512G	1T
15	CAG	GENERATION @ production ramp (3-Year Production Start Cycle)	64M				256M			1G		4G			16G		
16	CAG	GENERATION @ samples/introducer (bits)	2.7E+08		5.4E+08		1.1E+09	2.1E+09	4.3E+09	8.6E+09	1.7E+10	3.4E+10	6.9E+10	1.4E+11	2.7E+11	5.5E+11	1.1E+12
17	CAG	GENERATION @ production ramp (bits)	6.7E+07		1.1E+08		2.7E+08		1.1E+09		1.3E+09		4.3E+09		1.7E+10		1.7E+10
18	CAG	Bits/cm2 @ sample/introduction	9.6E+07		1.6E+08		2.7E+08	4.6E+08	7.7E+08	1.3E+09	2.2E+09	3.7E+09	6.1E+09	1.0E+10	1.7E+10	2.9E+10	4.8E+10
19	CAG	"Affordable" cost/bit @ (packaged - microcents) @ samples/introduction	120		69		40	24	15	8.9	5.3	3.2	1.9	1.1	0.66	0.39	0.23
20		Logic (High-Volume: Microprocessor)															
21	CAG	Logic transistors/cm2 (packed, including on-chip SRAM)	3.7E+06		4.8E+06		6.2E+06	1.1E+07	1.8E+07	2.6E+07	3.9E+07	5.7E+07	8.4E+07	1.2E+08	1.8E+08	2.6E+08	3.9E+08
22	CAG	Affordable cost/transistor @ (packaged - microcents)	3000		2281		1735	1003	580	385	255	167	110	74	50	33	22
23		Logic (Low-Volume: ASIC)															
24	Design TWG	Usable transistors/cm2 (auto layout)	8.0E+06		1.1E+07		1.4E+07	1.8E+07	2.4E+07	3.1E+07	4.0E+07	5.1E+07	6.4E+07	8.0E+07	1.0E+08	1.3E+08	1.6E+08
25	Design TWG	Non-recurring engineering cost/usable transistor (microcents)	50		35		25	19	15	12	10	7	5	4	2.5	1.8	1.3
26		Number of Chip I/Os															
27	AP/Design TWG	Chip-to-package (pads) high-performance	1450		1703		2000	2449	3000	3464	4000	4648	5400	6279	7300	8485	9862
28	AP/Design TWG	Chip-to-package (pads) cost-performance	800		883		975	1193	1460	1696	1970	2287	2655	3085	3585	4164	4836
29		Number of Package Pins/Balls															
30	AP/Design TWG	Microprocessor/controller, cost-performance	600		697		810	944	1100	1285	1500	1732	2000	2324	2700	3127	3622
31	AP/Design TWG	ASIC (high-performance)	1100		1285		1500	1817	2200	2569	3000	3507	4100	4749	5500	6400	7447
32		Cost-Per-Pin															
33	AP TWG	Package cost (cents/pin) (cost-performance) - minimum	2.80		2.52		2.27	2.05	1.86	1.72	1.59	1.48	1.37	1.27	1.17	1.08	1.00
34	AP TWG	Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)	1.40		1.21		1.04	0.93	0.83	0.78	0.73	0.68	0.63	0.58	0.54	0.50	0.46
35	Genda Hu/ERSO	Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)			1.00		0.90	0.80	0.80	0.80							
36		Chip Frequency (MHz)															
37	Design TWG	On-chip local clock, (high performance)	750		968		1250	1620	2100	2711	3500	4583	6000	7746	10000	13001	16903
38	Design TWG	On-chip, across-chip clock (high performance)	750		949		1200	1386	1600	1789	2000	2236	2500	2739	3000	3320	3674
39	Design TWG	On-chip, across-chip clock, high-performance ASIC (new line item)	300		387		500	592	700	794	900	1039	1200	1342	1500	1704	1936
40	Design, TWG	On-chip, across-chip clock (cost-performance)	400		490		600	693	800	938	1100	1241	1400	1587	1800	2036	2303
41																	
42	Design TWG	Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)	750		949		1200	1386	1600	1789	2000	2236	2500	2739	3000	3320	3674
43		Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	250		346		480	652	885	957	1035	1153	1285	1407	1540	1701	1878
44		Chip Size (mm2) (@sample/introduction)															
45	CAG	DRAM	280		335	569	400	473	560	665	790	941	1120	1330	1580	1879	2234
46	CAG	Microprocessor	300		319		340	382	430	473	520	568	620	682	750	822	901
47	Des. TWG/PIDS	ASIC [max litho field area]	480		620		800	849	900	949	1000	1049	1100	1196	1300	1388	1482
48																	
49	Litho TWG	Maximum Lithographic Field Size - Area (mm2)	484		622		800	849	900	949	1000	1049	1100	1196	1300	1388	1482
50	Litho TWG	Maximum Lithographic Field Size - Width (mm)	22		27		32	34	36	38	40	42	44	48	52	56	59
51	Litho TWG	Maximum Lithographic Field Size - Length (mm)	22		23		25	25	25	25	25	25	25	25	25	25	25
52	Interconnect TWG, PIDS	Maximum Number Wiring Levels - maximum	6		6		7	7	7	7	8	8	9	9	9	9	10
53	Interconnect TWG, PIDS	Maximum Number Wiring Levels - minimum	6		6		6	6	7	7	7	7	8	8	9	10	10
54		Defect Reduction															
55	Defect Reduc.Technol.TWG	DRAM 1st Year Electrical DO @ 60% Yield (d/m2)	2080		1740		1455	1230	1040	874	735	618	520	439	370	312	263
56	Defect Reduc.Technol.TWG	DRAM 3rd Year Electrical DO @ 80% Yield (d/m2)	1390		1170		985	827	695	584	490	414	350	296	250	211	179
57	Defect Reduc.Technol.TWG	MPU 1st Year Electrical DO @ 60% Yield (d/m2)	1940		1821		1710	1522	1355	1232	1120	1026	940	854	775	707	645
58	Defect Reduc.Technol.TWG	MPU 3rd Year Electrical DO @ 80% Yield (d/m2)	1310		1227		1150	1023	910	832	760	697	640	580	525	479	436
59	Defect Reduc.Technol.TWG	ASIC 1st Year Electrical DO @ 60% Yield (d/m2)	1210		937		725	684	645	612	580	554	530	488	450	422	396
60																	
61	PIDS	Minimum, mask count - maximum	22		23		24	24	24	25	26	27	28	28	28	29	29
62	PIDS	Minimum, mask count - minimum	22		22		22	23	24	24	24	25	26	27	28	29	30
63		Maximum substrate diameter (mm)															
64	CAG, FI, I300I	Bulk or epitaxial or SOI*** wafer	200		200		300	300	300	300	300	300	300	300	300	300	450
65		Power Supply Voltage (V)															
66	PIDS	Minimum logic Vdd (V) - maximum [for maximum performance]	2.5		2.1		1.8	1.6	1.5	1.3	1.2	1.0	0.9	0.7	0.6	0.50	0.42
67	PIDS	Minimum logic Vdd (V) - minimum [for lowest power]	1.8		1.7		1.6	1.4	1.2	1.0	0.9	0.7	0.6	0.5	0.5	0.43	0.37
68		Maximum Power															
69	AP TWG	High-performance with heatsink (W)	70		79		90	108	130	144	160	165	170	172	175	179	183
70	AP TWG	Battery (W) - (Hand-held)	1.2		1.3		1.4	1.7	2.0	2.2	2.4	3	2.8	3.0	3.2	3.4	3.7
71		Test															
72	Test TWG	Volume tester cost/pin (\$K/pin) (high-performance)	10		9		8	7	6	5	5	5	5	5	5	5	5
73	Test TWG	Volume tester cost/pin (\$K/pin) (cost-performance)	5		4		4	3	3	2	2	2	2	2	2	2	2
74																	
75																	
76																	
77																	
78																	
79		***Silicon On Insulator															
80																	

	A	B	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF
1		INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS															
2		Overall Technology Characteristics Table B-1 (Rev 2.3f IRC Proposal 11/30/98)															
3		Table B-1 [Multiple Year/Inter-Generation Data]															
4																	
5																	
6		PROPOSED TECHNOLOGY NODE DESIGN RULE:															
7		[NEC (Nikkei Microdevices, 9/98)]:															
8		Proposed [1999b - (2yr)] [incl.1998 update, 10/98]															
9		Table Line Item Name:															
10		Table Line Item Owner(s):															
11		YEAR OF FIRST PRODUCT SHIPMENT															
12		TECHNOLOGY GENERATIONS (nm) DENSE LINES (DRAM Half-Pitch)															
13		TECHNOLOGY GENERATIONS (nm) ISOLATED LINES (Logic Gates)															
14		TECHNOLOGY GENERATIONS (nm) Logic Half-Pitch															
15		Memory															
16		GENERATION @ samples/introducer (2-Year Introduction Cycle)															
17		GENERATION @ production ramp (3-Year Production Start Cycle)															
18		GENERATION @ samples/introducer (bits)															
19		GENERATION @ production ramp (bits)															
20		Bits/cm2 @ sample/introduction															
21		*Affordable* cost/bit @ (packaged - microcents) @ samples/introduction															
22		Logic (High-Volume: Microprocessor)															
23		Logic transistors/cm2 (packed, including on-chip SRAM)															
24		Affordable cost/transistor @ (packaged - microcents)															
25		Logic (Low-Volume: ASIC)															
26		Usable transistors/cm2 (auto layout)															
27		Non-recurring engineering cost/usable transistor (microcents)															
28		Number of Chip I/Os															
29		Chip-to-package (pads) high-performance															
30		Chip-to-package (pads) cost-performance															
31		Number of Package Pins/Balls															
32		Microprocessor/controller, cost-performance															
33		ASIC (high-performance)															
34		Cost-Per-Pin															
35		Package cost (cents/pin) (cost-performance) - minimum															
36		Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)															
37		Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)															
38		Chip Frequency (MHz)															
39		On-chip local clock, (high performance)															
40		On-chip, across-chip clock (high performance)															
41		On-chip, across-chip clock, high-performance ASIC (new line item)															
42		On-chip, across-chip clock (cost-performance)															
43		Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)															
44		Chip-to-board (off-chip) speed (high-performance, for peripheral buses)															
45		Chip Size (mm2) (@ sample/introduction)															
46		DRAM															
47		Microprocessor															
48		ASIC [max litho field area]															
49		Maximum Lithographic Field Size - Area (mm2)															
50		Maximum Lithographic Field Size - Width (mm)															
51		Maximum Lithographic Field Size - Length (mm)															
52		Maximum Number Wiring Levels - maximum															
53		Maximum Number Wiring Levels - minimum															
54		Defect Reduction															
55		DRAM 1st Year Electrical DO @ 60% Yield (d/m2)															
56		DRAM 3rd Year Electrical DO @ 80% Yield (d/m2)															
57		MPU 1st Year Electrical DO @ 60% Yield (d/m2)															
58		MPU 3rd Year Electrical DO @ 80% Yield (d/m2)															
59		ASIC 1st Year Electrical DO @ 60% Yield (d/m2)															
60		Minimum, mask count - maximum															
61		Minimum, mask count - minimum															
62		Maximum substrate diameter (mm)															
63		Bulk or epitaxial or SOI*** wafer															
64		Power Supply Voltage (V)															
65		Minimum logic Vdd (V) - maximum [for maximum performance]															
66		Minimum logic Vdd (V) - minimum [for lowest power]															
67		Maximum Power															
68		High-performance with heatsink (W)															
69		Battery (W) - (Hand-held)															
70		Test															
71		Volume tester cost/pin (\$K/pin) (high-performance)															
72		Volume tester cost/pin (\$K/pin) (cost-performance)															
73		***Silicon On Insulator															