Design DTWG for 1999 ITRS

January 8, 1999

Members

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TBD	

Design Environment

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Our Past

- Members “recruited”
- Two conference calls
- Revision of Table 7
- TWG web site set up
- Assignments of text, figures, liaisons

Our Future Schedule

- 01/15/99 First pass text and figures due
- 01/19/99 Conference call 1-3pm EST
- 02/18/98 Face-to-face working meeting on tables, figures, text, San Francisco (incl ITWG)
- 03/01/98 Revised draft of text, tables, figures due
- 03/15/98 Comments on revisions due
- 03/31/98 Text, tables, figures to RCG
- 07/09/98 Roadmap workshop

Table 7 - Design & Test Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 NM / BEFORE 2006	
Silicon complexity	Large numbers of interacting devices and interconnects Atomic-scale effects Impact of signal integrity, noise, reliability, manufacturability Need for new logic families to meet performance challenges Power and current management; voltage scaling Alternative technologies (e.g. copper, low-K, SOI)
System complexity	Greatly increased system and function size System-on-a-chip design with a diversity of design styles (including analog, mixed signal, RF, MEMS, electro-optical) RF issues Integrated passive components Embedded software as a key design problem
Design procedure complexity	Interacting design levels with multiple, complex design constraints Convergence and predictability of design procedure Specification and estimation needed at all levels Technology remapping or migration to maintain productivity Core-based, IP-reused designs and standards for integration Large, collaborative , multi-skilled, geographically distributed teams
Verification complexity	Timing and function co-verification System-level formal verification/specification Core-based design verification (including analog/mixed signal) Verification of complex processors and architectures
Test/testability complexity	Quality and yield impact due to test equipment limits Test of core-based designs from multiple sources (including analog, RF) Difficulty of at-speed test with increased clock frequencies Signal integrity testability

Table 7 - Design & Test Difficult Challenges

FIVE ADDITIONAL DIFFICULT CHALLENGES < 100 nm / BEYOND 2006	
Silicon complexity	Design with novel devices (multi-threshold, 3D layout, SOI, etc.) Soft errors Increasing uncertainty in fundamental chip parameters (e.g. signal skew)
System complexity	Total system integration including new integrated technologies (e.g. MEMS, electro-optical, electro-chemical, electro-biological) Design techniques for fault tolerance Embedded software and on-chip operating system issues
Design procedure complexity	True incremental, one-pass design process Integration of design process with manufacturing to address reliability and yield
Verification complexity	Verification of heterogeneous systems (including mixed-signal and MEMS)
Test/testability complexity	Greatly increased dependence on self-test solutions System test (including MEMS and electro-optical components)

Changes from 1997 NTRS

- Relate “potential solutions” figures to “difficult challenges”
- Use meaningful figures:
  - “speed/performance issue”
  - “productivity gap”
  - “D&T technology requirements”
- Replace “laundry list” of needs by:
  - specific priorities (what, when, why, cost, consequences)
  - specific bottlenecks
- Replace “ASIC” by “SOC” as key driver
- Expose new challenges:
  - embedded software
  - importance of analog/mixed signal/CMOS RF

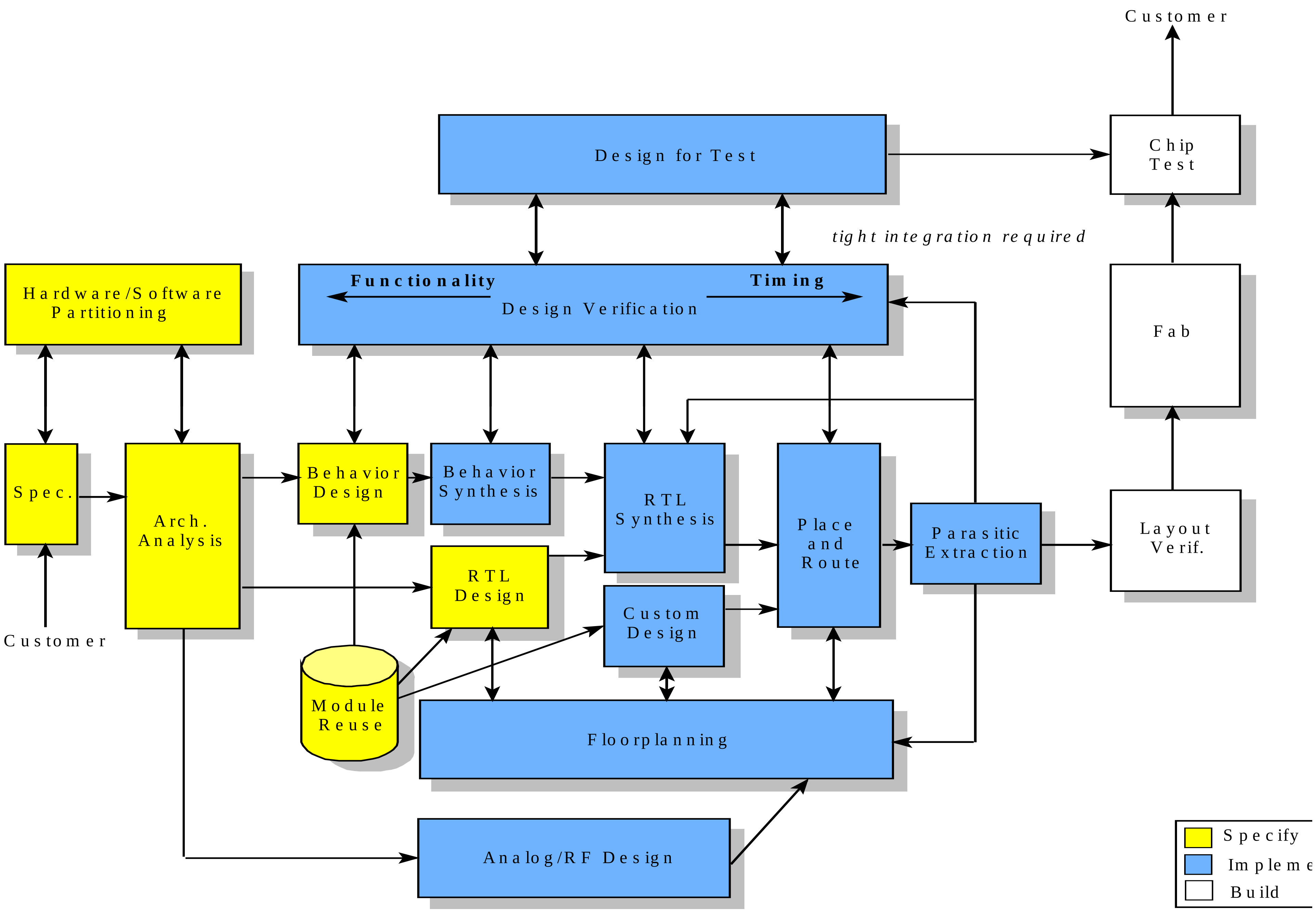


Figure 4 Overall Design and Test Flow

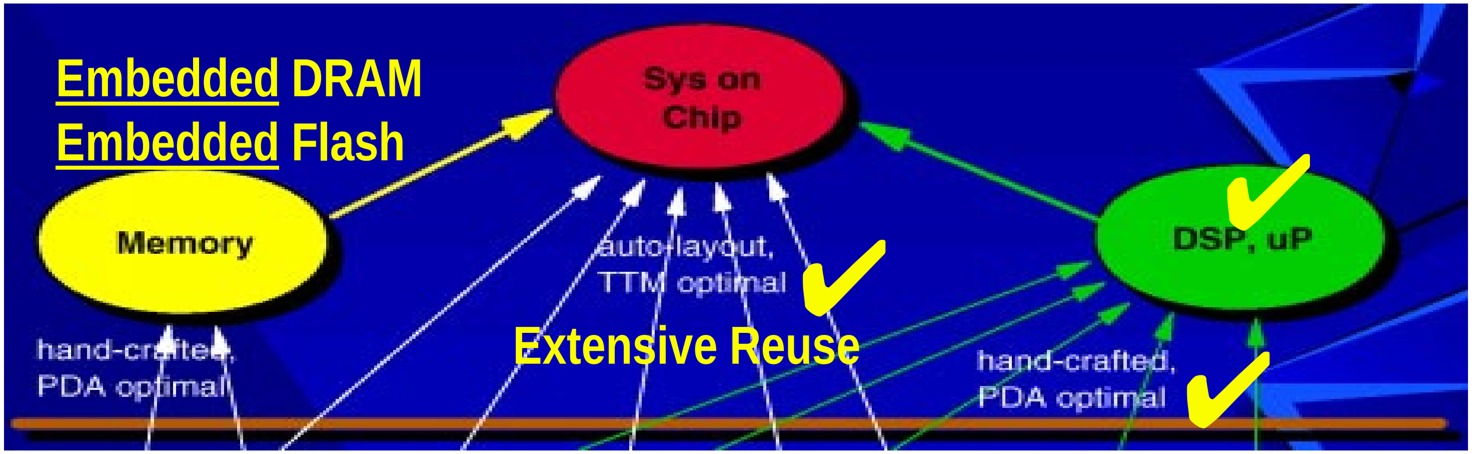
International Feedback

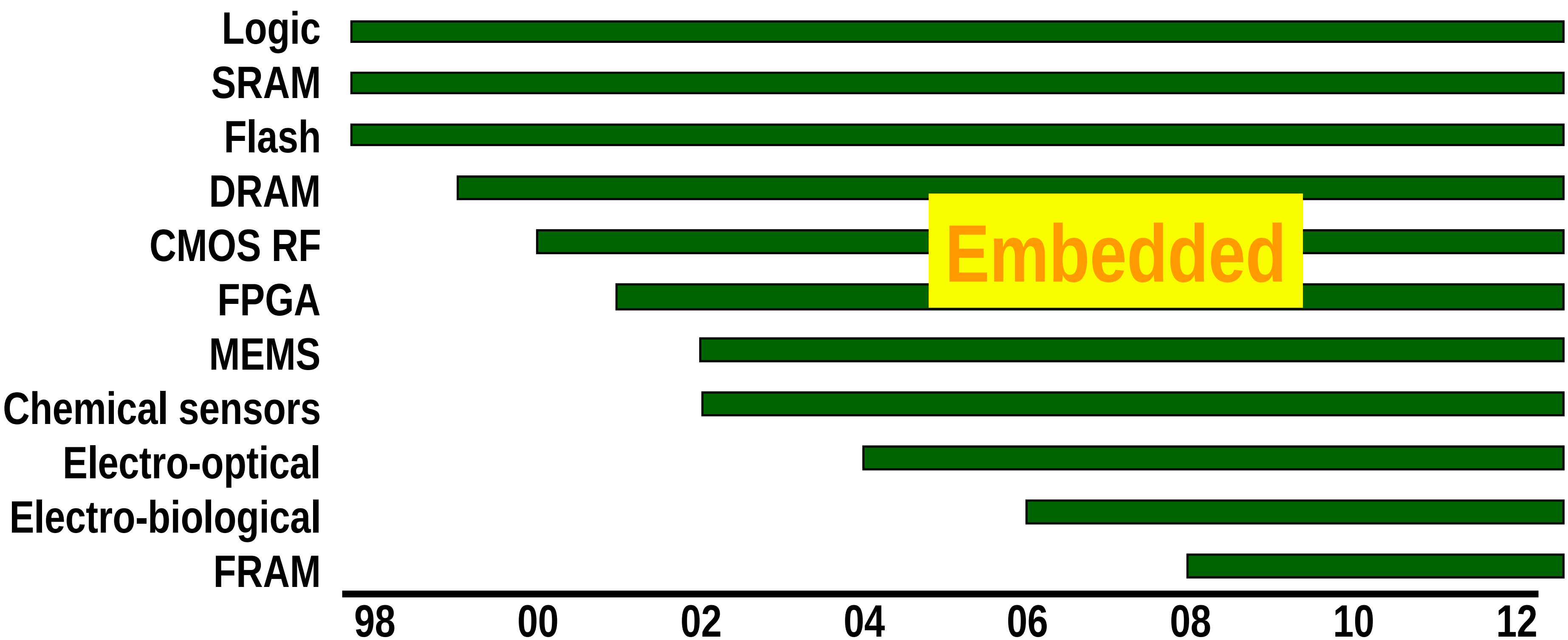
- Importance of System-on-a-Chip not well-reflected in the 1997 NTRS
  - ASIC category is outdated and irrelevant
  - “It is better to define the target product and its profile” (EIAJ/STRJ-WG1)
  - “A roadmap must make sense business-wise” (STRJ)
- Importance of Analog/Mixed Signal/CMOS RF not well-reflected in the 1997 NTRS
- We really need to focus on a Design Productivity Metric
  - Needed to explain the importance of reuse
  - Some data available (e.g. “design productivity gap” slide)
- Roadmap does not adequately reflect the role of, and design challenges associated with, embedded software and its interaction with hardware

Specific Recommendations

- We must change the ASIC category to System-on-a-Chip throughout the Roadmap as soon as possible
- The category should be motivated primarily by economic factors and their implications
- The category will include challenges in the “Embedded-*” categories: where * = DRAM, analog, RF, …, software.
- It will have significant implications for other areas, especially design, packaging, test, interconnect (e.g. power issues)

Importance of System-On-A-Chip





Importance of System-on-a-Chip
(called *System LSI* in Japan)

- *Could* be the most important category to the overall semiconductor industry in the years ahead
- Not the largest chips! Driven by economic rather than technological factors
- Drives technology in the mixed-technology areas
  - Embedded DRAM, flash, FPGA, analog, CMOS RF, ...
- Drives packaging and test emphasis in significantly different directions
- Drives design technology
  - Design reuse, heterogeneous systems, embedded software
  - EDA- Energy/Delay/Area optimization

Approach to Analysis for SOC

Start Here ➡ $$ Categories: (e.g. $1, $3, $10, $30, $100)

Packaging (40%?)

Test (30%?)

How many $$ left?

How complex a chip can I afford?

What can I build?

Mixed technologies

Semiconductor ITRS projections

Design reuse

3 Requirements for EDA Technology

The purpose of this chapter is to specify the environment that surrounds the EDA technology. To be more specific, we will define a system LSI called Cyber-Giga-Chip as a design target and analyze the demand for EDA technology .

3.1 Profile of Cyber-Giga-Chip

The specification of the system LSI for specific uses in 2002 is defined based on these investigation results. It is called Cyber-Giga-Chip, abbreviated as CGC. CGC, whose profile is shown in Figure 5, consists of such cores as CPU, DSP, memory, and so on, and memory/ logic consolidation technology and digital/ analog consolidation technology are important.

Figure5 Cyber-Giga-Chip

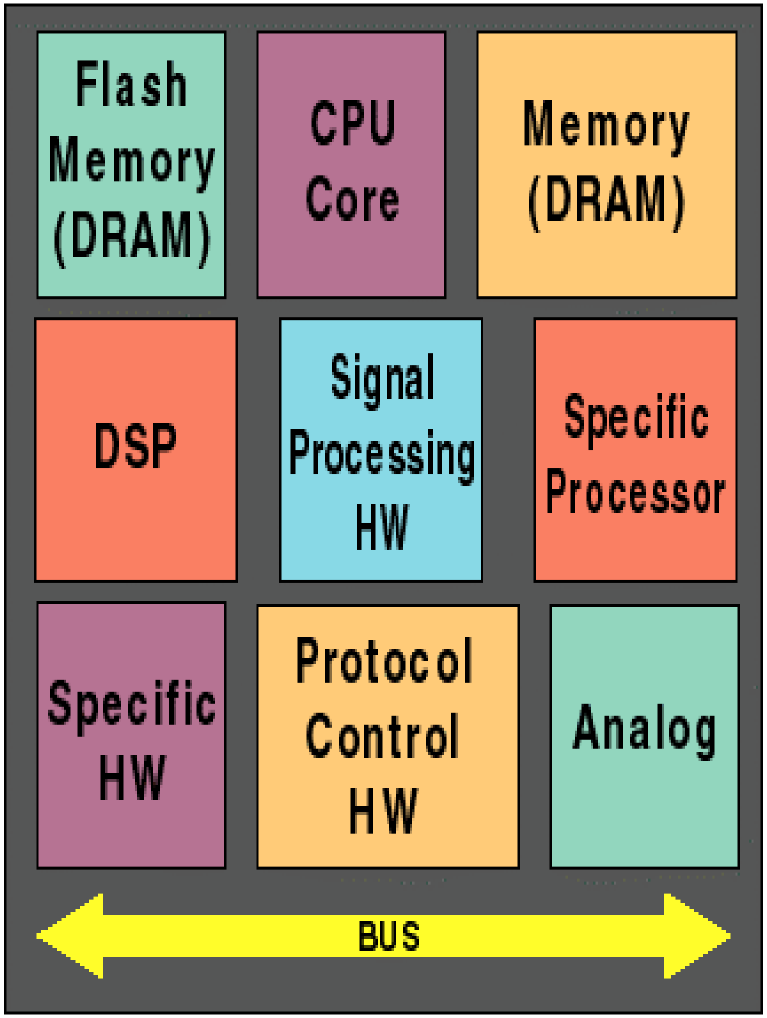
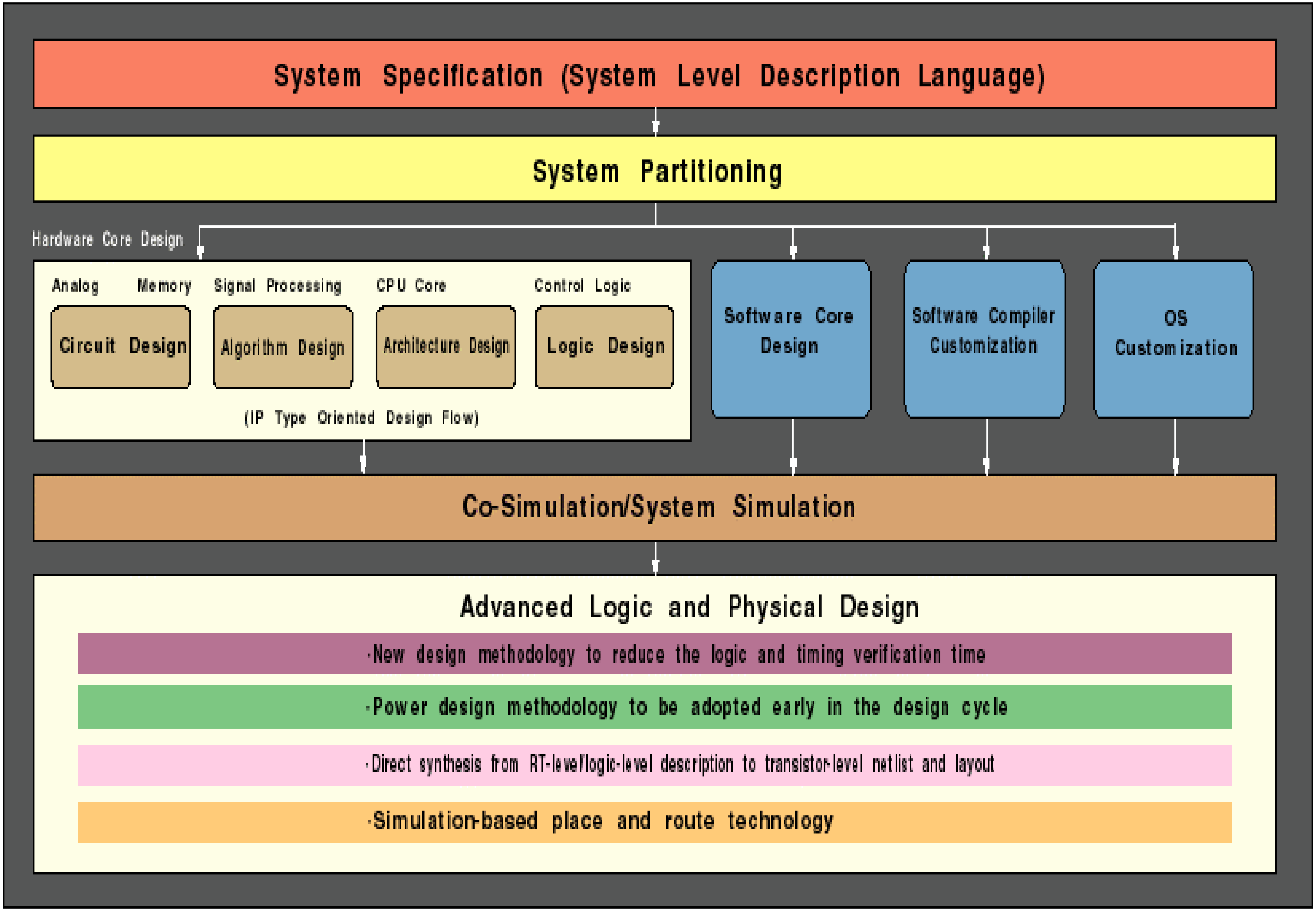


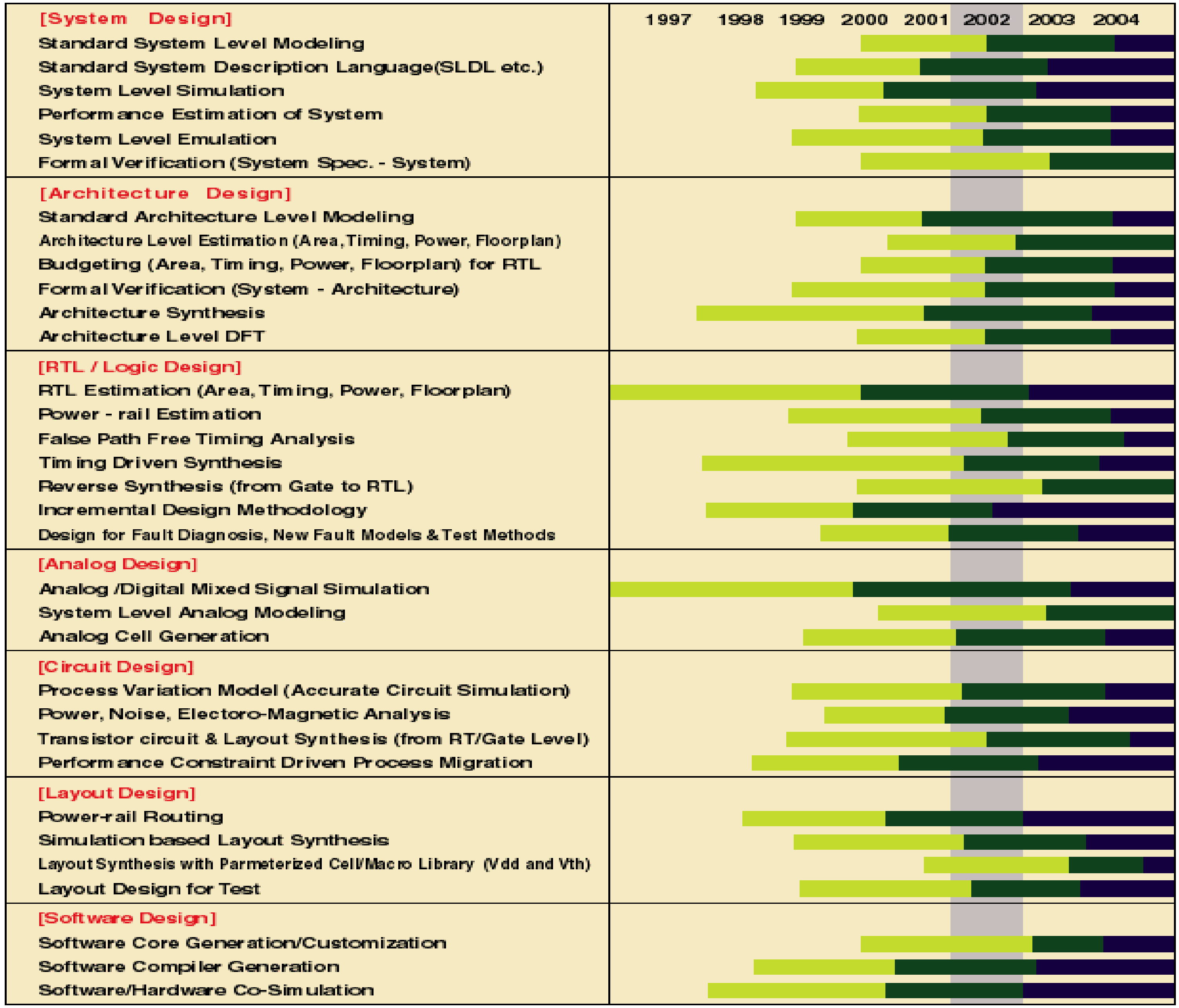
Figure 7 Cyber-Giga-Chip Design Flow in year 2002



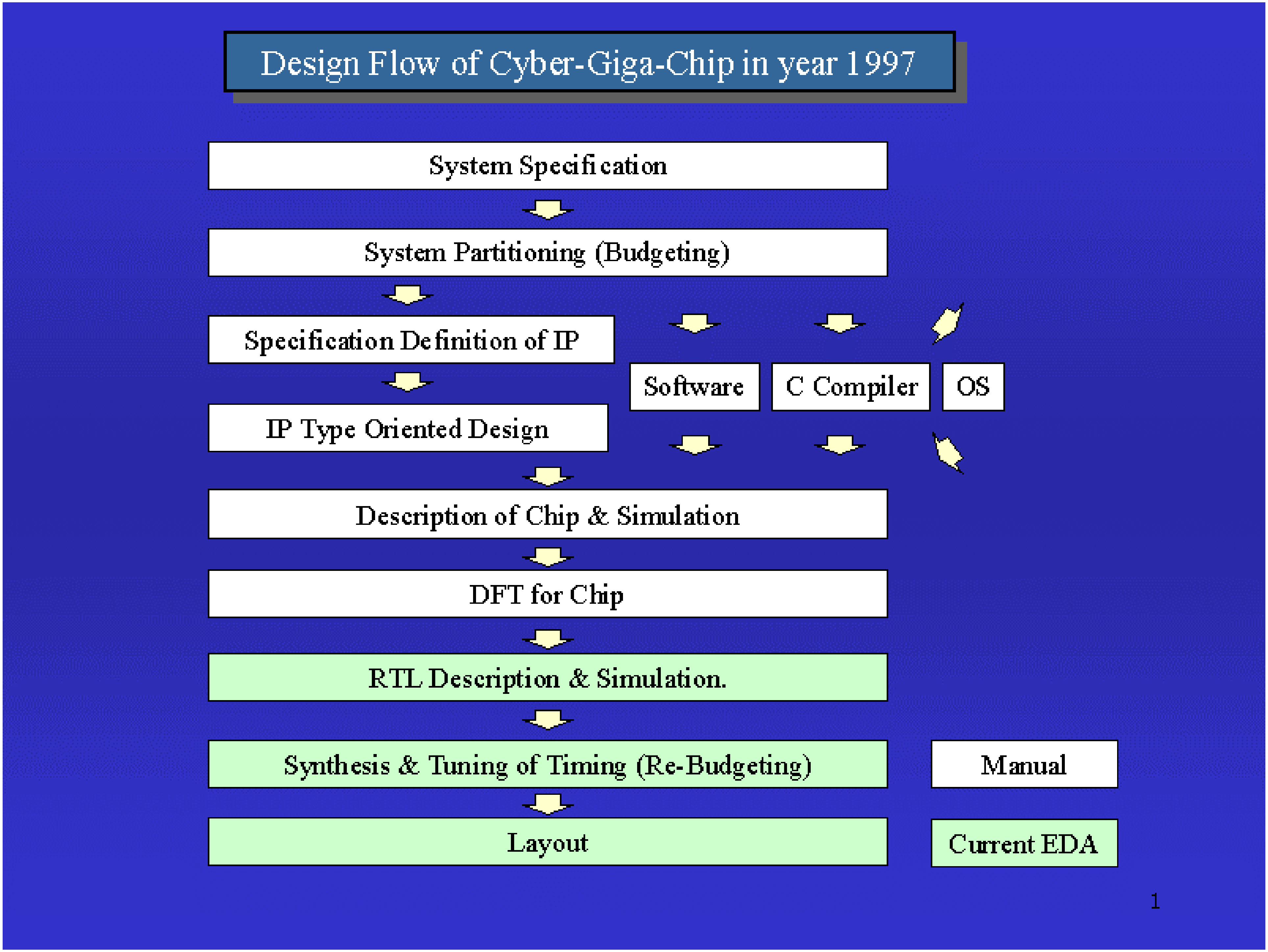
5.1.2 EDA Technology Roadmap for Cyber-Giga-Chip

Table 19 and Table 20 show EDA Technologies to make the design of Cyber-Giga-Chip efficient and how it changes in next five years and later.

Table 19, and Table 20 Transition of EDA Technology

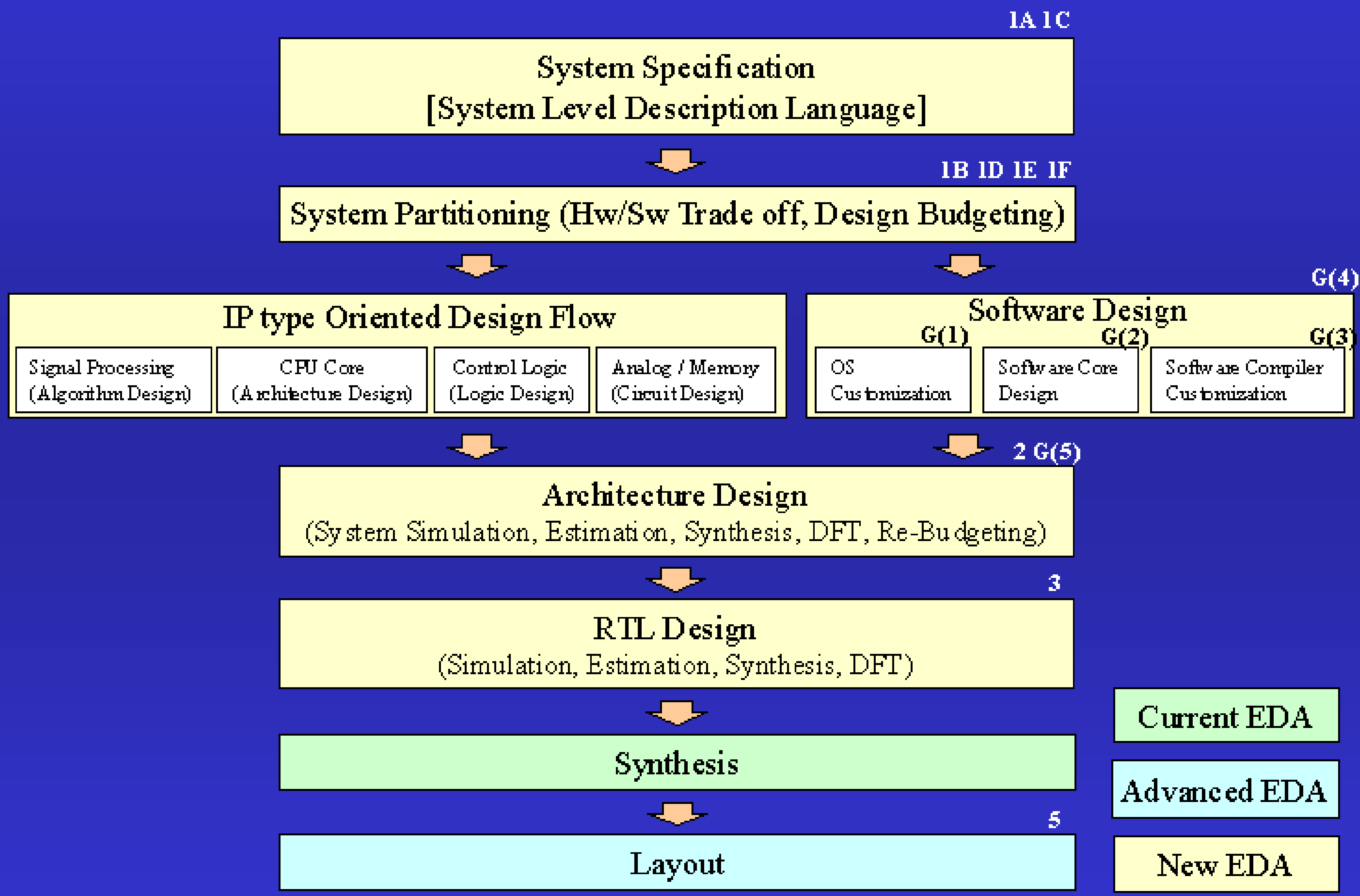


development
early adoption
widely applied

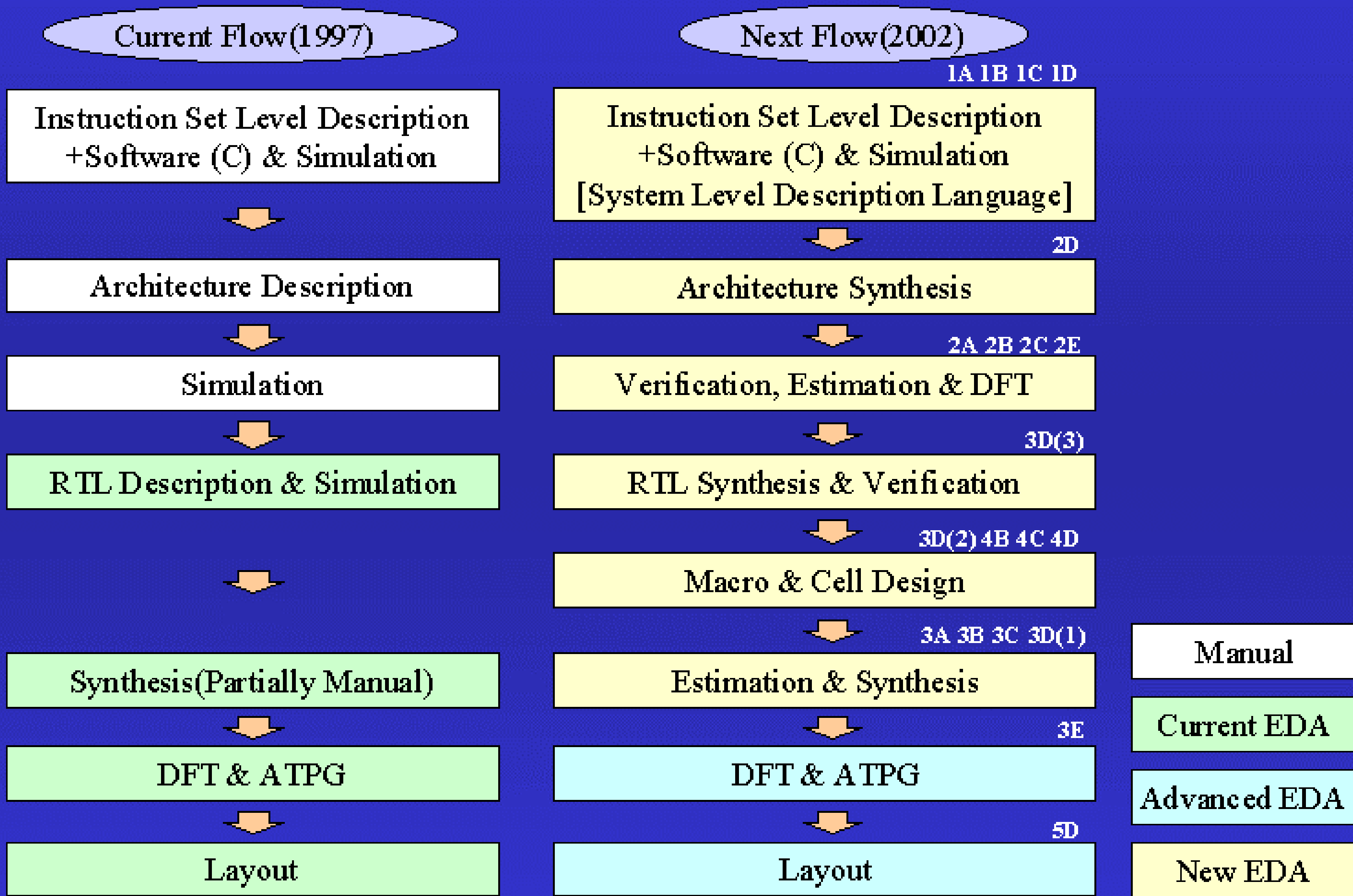


Design Flow of Cyber-Giga-Chip in year 1997
System Specification
System Partitioning (Budgeting)
Specification Definition of IP
IP Type Oriented Design
Software
C Compiler
OS
Description of Chip & Simulation
DFT for Chip
RTL Description & Simulation.
Synthesis & Tuning of Timing (Re-Budgeting)
Layout
Manual
Current EDA

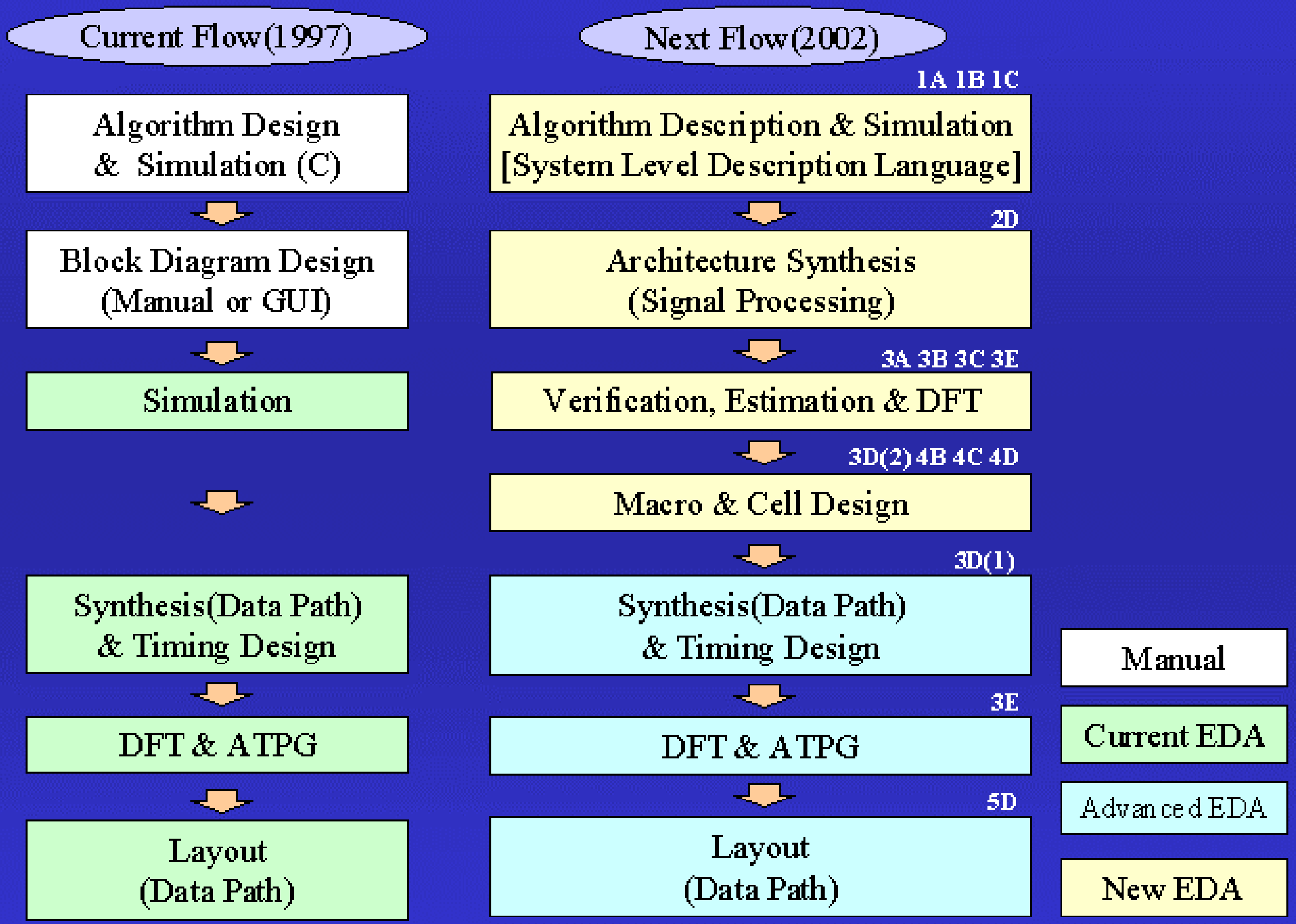
Design Flow of Cyber-Giga-Chip in year 2002



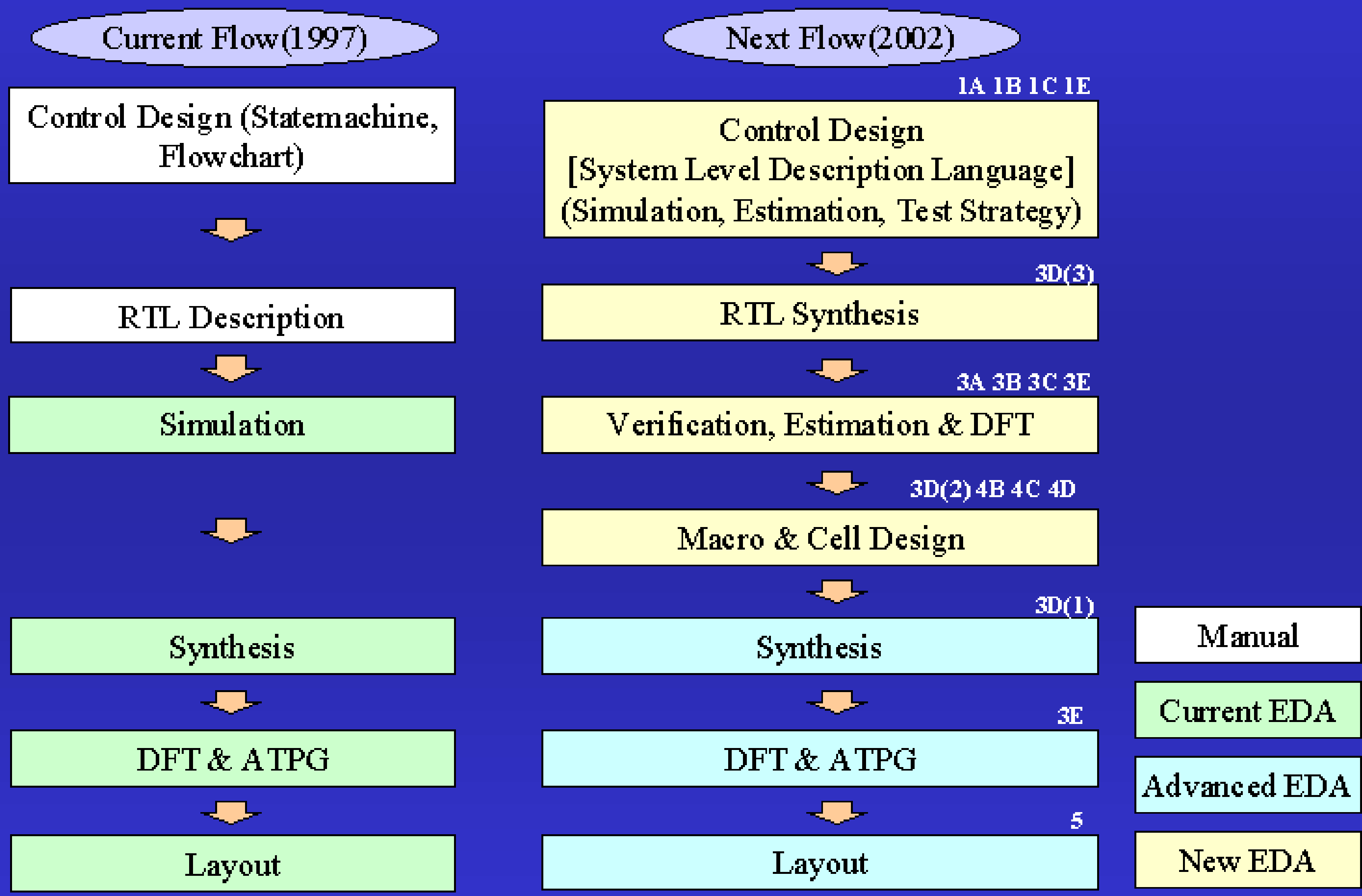
Design Flow of CPU Cores



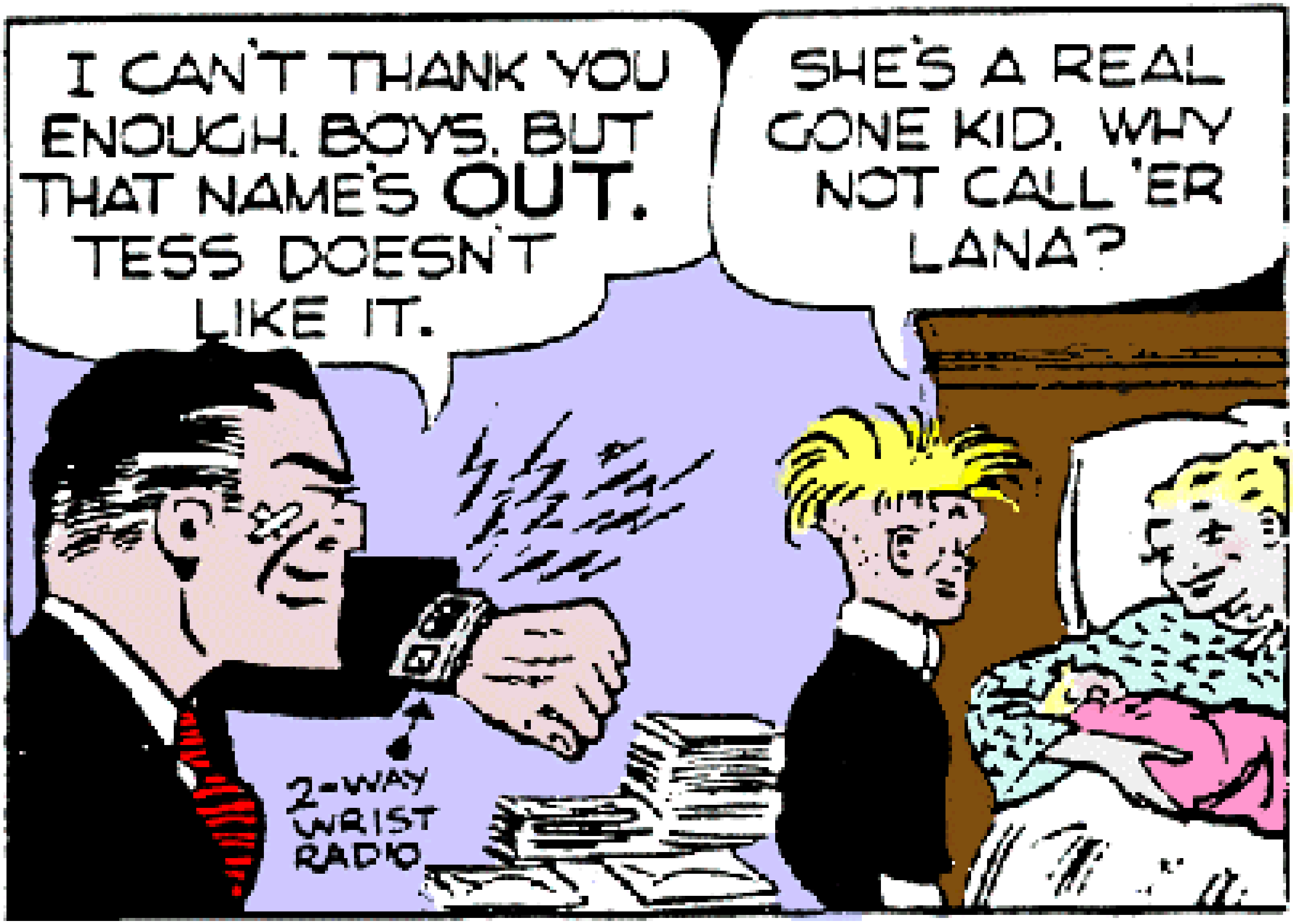
Design Flow of Digital Signal Processing Cores



Design Flow of Controller Cores



2-Way Wrist Radio -- The Vision in 1946



Dick Tracy May 20, 1951 Tribune Media Services


Have you ever installed a Video phone on your wrist?
Features:
• Audio/video Answering Machine (30 min. audio/10 min. video)
• One day between recharge (6.5 hours of continuous use)
• Speech Recognition (digits, commands and names)
• Visual communication (incl. camera)
• Full-duplex Speakerphone
• Cellular Videophone
• Watch
Lucent Technologies
Bell Labs Innovations