ERD Chapter review
Logic and information processing

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Exploratory Hybrid Electronic Device Lab.
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<td>추석, 9/14 - no class, 9/23 보강</td>
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<td>Week 3 (9/19, 21)</td>
<td>History of semiconductor device: from 90’s to present,</td>
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<td>Week 5 (10/3, 5)</td>
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* Class notes, references and other notices will be posted at [http://www.gistexel.com/PDS/postCMOS device technology](http://www.gistexel.com/PDS/postCMOS device technology)
Chapter list

4.2 Logic devices

4.2.4.4 MOSFET: extending MOSFETs to the end of the roadmap
  4.2.4.4.1 CNT FET (5)
  4.2.4.4.2 GNR FET (6)
  4.2.4.4.3 NW FET (4)
  4.2.4.4.4 n-type III-V channel replacement device (1)
  4.2.4.4.5 n-type Ge channel replacement device (2)
  4.2.4.4.6 tFET (3)

4.2.4.5 Charge based beyond CMOS: non-conventional FETs and other charge based information carrier devices
  4.2.4.5.1 Spin FET and spin MOSFET transistor (is this charge based? move to next section?)
  4.2.4.5.2 IMOS (more suitable for extending MOSFET)
  4.2.4.5.3 Negative gate capacitance FET
  4.2.4.5.4 NEMS switch (NEM switch and NEM FET should be differentiated)
  4.2.4.5.5 Atomic switch
  4.2.4.5.6 Mott FET

4.2.5 Alternative information processing devices
  4.2.5.4 Non-FET, Non charge based “beyond CMOS” devices
    4.2.5.4.1 Spin wave devices
    4.2.5.4.2 Nanomagnetic logic
    4.2.5.4.3 Exitonic field effect transistor
    4.2.5.4.4 BisFET
  4.2.5.4.5 Spin torque majority logic gate
  4.2.5.4.6 All spin logic

• Survey, assess, catalog viable new information devices
CNTFET

• *Even though significant progress has been made, the ultimate goal of depositing dense, aligned, and only semiconducting nanotubes as a high mobility channel replacement material on a silicon wafer remains elusive*

• Agree with this statement, but then why put this section first?

R. Chau et al., ITN, 05
GNRFET

- Too much focus on the summary of mobility
- Not much review on FET implementation issues (due to limited publications?)
  - Summary of requirements might be useful to readers and research groups
- Missing assessments on
  - Mobility extraction methodology
  - Device instability issues (hysteresis)
  - Effect of self heating
  - Noise characteristics

J. Martin et al., Nature Physics, 2008
NWFET

• Section on nanowire FET is too short
• Missing assessment on pros, cons, benchmarking, mostly a brief summary
• Didn’t go through a table, but pros/cons table might be useful for next version
III-V FET

- Title, "n-type III-V channel", seems to be wrong
- Summary on performance only
- Status review on the requirements suggested in this section would be useful next time
  
  - The major challenges facing high volume production of III-V devices include the need for high quality, low EOT gate dielectrics, damage-free low resistivity junctions, and hetero-integration on a VLSI compatible silicon substrates.

- Why n-type channel only while including p-channel device works also?
- Need more comments/ assessment on 3D integration aspects in future
Ge FET

- Title, “n-type Ge channel”, seems to be wrong. There are strong works going on Ge nMOS side also.

- Very subjective assessment?
  - In summary, even though additional progress is required in reducing EOT, continuing gate-length scaling to and below 20nm, and development of lower-resistivity diffusion layers with lower-resistivity metal contacts, Ge n-channel MOSFETs are good potential candidates to extend CMOS to the end of the Roadmap.

- Need more concrete review on EOT, doping profile control, 3D compatibility next time
tFET

• Very good summary
• tFET is good for swing reduction and there are intensive research going on, but too much focus on on/off ratio control
• tFET is not a savior for power management problem

• ERD section in general seems to miss an overall view on power problem
• tFET can improve power consumption in FEOL which is a minor portion of power consumption problem
• Section or table comparing the impact of each technology on overall chip level performance would be nice

Over 50% of the dynamic power results from interconnections switching, the gates contribute another 34% and the rest is diffusions.

SpinFET

- No discussion on figure of merit
- No clear explanation on the difference between spinFET, spin MOSFET
  - *Field-effect spin-transistors can be divided into two categories, i.e., spin-FET and spin-MOSFET. Although these device structures are similar, their operating principles are quite different.*

- Missing assessment on the requirements for spinFET: what are the features that spinFET should improve or demonstrate

- Typo in the page “ffunctionalities”
IMOS

- Limit of IMOS has been presented.
  - Low voltage operation impossible
  - Reliability is an intrinsic problem
- Should be dropped from an option?

- Impact ionization coefficient saturates at high field
- Short channel device doesn’t have enough distance to get the impact ionization
- Device below 50nm would not be functional
- Need a smaller gap impact ionization medium like Ge channel
- Device operation window is too narrow to be practical

A. Savio et al, TED, 56(5), p.1110, 2009

$V_{DS}=6\text{V}$

$V_{DS}=5.1\text{V}$

$V_{DS}=6\text{V}$

$V_{DS}=6.0\text{V}$

$V_{DS}=5.3\text{V}$

$V_{DS}=6.3\text{V}$

$V_{DS}=5.4\text{V}$

$V_{DS}=6.6\text{V}$

$V_{DS}=5.7\text{V}$

$V_{DS}=6.0\text{V}$

$V_{DS}=6.3\text{V}$

$V_{DS}=6.6\text{V}$

$V_{DS}=5.7\text{V}$

A. Savio et al, TED, 56(5), p.1110, 2009
Negative capacitance FET

• Very good summary on development status
• Physical explanation is weak (due to limited space)
• “In principle, the scalability of the device should be similar to the one of a MOSFET” – probably wrong statement

• Ferroelectric capacitor in series of gate capacitance may improve swing mathematically, but it limits the speed of MOSFET to ferroelectric switching speed (from 1psec to ~30psec?)
• Need other performance specifications other than swing
  - Switching speed
NEMS

- NEMS switch vs NEM switch (O)
- NEM switch, NEM FET, which is a main concept? Not clear
- Wrong assessment on scalability. Reference 314 refers 15nm airgap, but device size is too big
- Most of materials are not scalable in 100nm range
- Works on graphene NEM switch is missing
- Concepts on NEMS-CMOS, Backend NEM switch device are not described clearly

Graphene
SW-CNT
Silicon
TiN

Max. gate swing range (nm)

Gate length (nm)
Atomic Switch

- Good and concise description. A little more explanation about the need for architectural options or states, challenges

  *In addition, development of the architecture for nonvolatile devices is desired same as with other nonvolatile logic devices.*

Mott FET

- Good description on physics
- device performance factors, current challenges and scalability are not discussed
4.2.5 Alternative information processing devices

**Spinwave device**
- Over head for encoder and decoder to interface with charge based circuit is not discussed

**Nano magnetic device**
- Over head for encoder and decoder to interface with charge based circuit is mentioned
- Need for interconnect architecture is also discussed (good description)
- Overhead for booster is a problem

**Exitonic FET**
- Success criteria are missing
4.2.5 Alternative information processing devices

**BisFET**
- Good idea, but even a single layer graphene FET has a lot of problem in an integration.
- Hard to imagine how this technology has any possible practical implications in future. Should a concept device be included?

**Spin torque majority logic gate**
- Even more conceptual than BisFET

**spin logic**
- Even more conceptual than STM logic gate
- Spin injection into metal/semiconductors – spin purity problem, development target or success criteria are not discussed

In general, these technologies are one step beyond the emerging devices. Even a success of emerging device is unclear at this point. I am concerned this list may give an wrong impression about the current crisis of device technology.
Devices/technologies missing in this section or desired for 2013 version

- In general, correlation between device and architecture are weak
  - Novel device technology can no longer be separated from architecture.
  - For example, discussion on the usefulness of reconfigurable architecture can be included in atomic switch and NEM switch section
- ERD expansion into BEOL to include 3D architecture: Non-charge based interconnect, atomic switch etc
- Separate section on hybrid devices might be useful: SET-MOS, SET-NEMS, CNT-NEMS, graphene NEMS
- Technology to reduce the device count (Ctot) may be worth to have separate attentions
  - Logic-MTJ hybrid or nonvolatile hybrid logic
  - Neuromorphic devices